**European Embedded Control Institute** 

**Graduate School on Control — Spring 2010** 

The Behavioral Approach to Modeling and Control

**Lecture IV** 





# First-principles models invariably contain latent (auxiliary) variables in addition to the (manifest) variables the model aims at.

In this lecture we study the emergence of latent variables and their elimination for LTIDSs.



# **The emergence of latent variables in physical models**

- Springs in series and in parallel
- A mechanical systems
- An RLC circuit
- The elimination theorem
- Modeling of RLC circuits using MNA (modified nodal analysis)

# Springs in series and in parallel

## **Interconnected springs**



#### **!!** Model the relation between *L* and *F* **!!**

#### **Interconnected springs**



#### **!!** Model the relation between *L* and *F* **!!**

**Typical force/length characteristic for a simple spring.** 





$$L_1 = \rho_1(F_1),$$
  $L_2 = \rho_2(F_2),$   
 $F = F_1 = F_2,$   $L = L_1 + L_2.$ 

(L,F): 'manifest',  $(L_1,F_1,L_2,F_2)$ : 'latent' variables.



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(*L*,*F*): 'manifest', (*L*<sub>1</sub>,*F*<sub>1</sub>,*L*<sub>2</sub>,*F*<sub>2</sub>): 'latent' variables. After elimination of the latent variables:  $L = \rho_1(F) + \rho_2(F)$ . Latent variables are easily eliminated in this case.



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**Linear springs:** 
$$L_1 = L_1^* + \rho_1 F_1, L_2 = L_2^* + \rho_2 F_2,$$
  
 $\rightsquigarrow \qquad L = L_1^* + L_2^* + (\rho_1 + \rho_2)F.$ 





$$L_1 = \rho(F_1), \qquad L_2 = \rho(F_2),$$
  
 $F = F_1 + F_2, \qquad L = L_1 = L_2.$   
 $(L,F)$ : 'manifest',  $(L_1,F_1,L_2,F_2)$ : 'latent' variables.





$$L_1 = \rho(F_1),$$
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 $F = F_1 + F_2,$   $L = L_1 = L_2.$ 

(L,F): 'manifest',  $(L_1,F_1,L_2,F_2)$ : 'latent' variables. After elimination of the latent variables:

$$\mathscr{B} = \{(L,F) \mid \exists \alpha : L = \rho_1(\alpha) = \rho_2(F - \alpha)\}$$

Latent variables are **not** easily eliminated in this case.





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  $L_2 = \rho(F_2),$   
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Latent variables are **not** easily eliminated in this case. Linear springs:  $L_1 = L_1^* + \rho_1 F_1, L_2 = L_2^* + \rho_2 F_2,$  $\sim L = \frac{\rho_2}{\rho_1 + \rho_2} L_1^* + \frac{\rho_1}{\rho_1 + \rho_2} L_2^* + \frac{\rho_1 \rho_2}{\rho_1 + \rho_2} F.$ 

## What springs teach us

- First principles models invariably contain latent variables, in addition the manifest variables the model aims at.
- It may be impossible to eliminate latent variables, even for simple models.
- Be careful about claiming what variable 'causes' what. For a simple spring we may think of the force as causing the length, but this situation is already not robust under parallel connection of two such springs.

## What springs teach us

- First principles models invariably contain latent variables, in addition the manifest variables the model aims at.
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We now illustrate the emergence and elimination of latent variables for a dynamical system.

# A mass-spring system

Two masses connected by a spring



Two masses connected by a spring



## View as interconnection of 3 systems.



# Now interconnect:



## **Constitutive equations:**

$$m_1 \frac{d^2}{dt^2} q_1 = F_1, \ m_2 \frac{d^2}{dt^2} q_2 = F_2, \ q_1' - q_2' = L^* - \rho F_1', \ F_1' = F_2',$$

with  $m_1$  and  $m_2$  the masses,  $\rho$  the elasticity coefficient of the spring, and  $L^*$  is equilibrium length. Assume that the spring operates in its linear regime.

# Now interconnect:



## **Constitutive equations:**

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**Interconnection equations:** 

$$F_1 = F_1', \ F_2 + F_2' = 0, \ q_1 = q_1', \ q_2 = q_2'.$$

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## **Constitutive equations:**

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#### **Interconnection equations:**

$$F_1 = F_1', \ F_2 + F_2' = 0, \ q_1 = q_1', \ q_2 = q_2'.$$

**Manifest variable:** 

$$\Delta = q_1 - q_2 - L^*.$$

## **Manifest behavior**



#### After elimination of the latent variables

 $F_1, F_2, F_1', F_2', q_1, q_2, q_1', q_2'$ , the following equation is obtained for the manifest variable  $\Delta$ 

$$\frac{m_1m_2}{m_1+m_2}\frac{d^2}{dt^2}\Delta + \frac{1}{\rho}\Delta = 0.$$

# An RLC circuit





#### **Model the port behavior of this circuit!**





#### **Model the port behavior of this circuit!**

**Manifest variables:** *V*, **the port voltage, and** *I*, **the port current.** 

$$\mathbb{T} = \mathbb{R}, \mathbb{W} = \mathbb{R}^2, w = \begin{bmatrix} V \\ I \end{bmatrix}.$$

**Choice of latent variables** 

To model this circuit, we use **nodal analysis**. Associate a digraph with the circuit:



**Latent variables: potentials** of vertices, currents in edges:  $(E_1, E_2, E_3, E_4), (I_a, I_b, I_c, I_d, I_e, I_f).$ 

TZOT	
	•
<b>NUL</b>	•

vertex 1:	$I_a + I_c + I_d = 0,$
vertex 2:	$I_c + I_e = 0,$
vertex 3:	$I_d + I_f = 0,$
vertex 4:	$I_b + I_e + I_f = 0.$

KCL:	vertex 1:	$I_a + I_c + I_d = 0,$
	vertex 2:	$I_c + I_e = 0,$
	vertex 3:	$I_d + I_f = 0,$
	vertex 4:	$I_b + I_e + I_f = 0.$
Constitutive	edge c:	$E_2-E_1=R_CI_c,$
equations:	edge d:	$E_3 - E_1 = L \frac{d}{dt} I_d,$
	edge e: (	$C\frac{d}{dt}(E_2 - E_4) = I_e,$
	edge f:	$E_3-E_4=R_LI_f.$

KCL:	vertex 1:	$I_a + I_c + I_d = 0,$
	vertex 2:	$I_c + I_e = 0,$
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equations:	edge d:	$E_3 - E_1 = L \frac{d}{dt} I_d,$
	edge e: $C\frac{d}{d}$	$\frac{d}{dt}(E_2 - E_4) = I_e,$
	edge f:	$E_3-E_4=R_LI_f.$
Manifest	port voltage:	$V = E_1 - E_4,$
variables:	port current:	$I = I_a$ .

In total, **10** latent variables:  $(E_1, E_2, E_3, E_4, I_a, I_b, I_c, I_d, I_e, I_f)$ , **2** manifest variables: (V, I),

and **10** equations.

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and **10** equations.

Which equations govern (V, I)?

A straightforward calculation (left as an exercise) leads to the following answer.

#### The port behavior is described by the following ODE:

 $\underline{\text{Case 1}}: \qquad CR_C \neq \frac{L}{R_L}$ 

$$\left(\frac{R_C}{R_L} + \left(1 + \frac{R_C}{R_L}\right)CR_C\frac{d}{dt} + CR_C\frac{L}{R_L}\frac{d^2}{dt^2}\right)V$$
$$= \left(1 + CR_C\frac{d}{dt}\right)\left(1 + \frac{L}{R_L}\frac{d}{dt}\right)R_CI$$

**Case 2:** 
$$CR_C = \frac{L}{R_L}$$

$$\left(\frac{R_C}{R_L} + CR_C \frac{d}{dt}\right) \mathbf{V} = \left(1 + CR_C \frac{d}{dt}\right) R_C \mathbf{I}$$

## The port behavior

- The behavioral equations after elimination tell *exactly* what the port behavior is. There are no hidden assumptions.
- Next, we prove that complete elimination of the latent variables is always possible in the class of linear constant coefficient differential equations.

It is a theorem!

The RLC circuit illustrates this in a particular example.

The different cases show that elimination is not a trivial matter. The order of the differential equation may chance with the element values, etc.

# **Representations of behaviors**

A model  $\mathscr{B}$  is a subset of a universum  $\mathscr{U}$ . There are many ways to specify a subset. For example,

- as the set of solutions of equations,
- as a projection.

**Kernels and projections** 

A model  $\mathscr{B}$  is a subset of a universum  $\mathscr{U}$ . There are many ways to specify a subset. For example,

as the set of solutions of equations:

$$f: \mathscr{U} \to \bullet, \qquad \mathscr{B} = \{ w \in \mathscr{U} \mid \frac{f(w)}{f(w)} = 0 \},$$

as a projection:

 $\mathscr{B}_{\text{extended}} \subseteq \mathscr{U} \times \mathscr{L},$ 

 $\mathscr{B} = \{ w \in \mathscr{U} \mid \exists \ \ell \in \mathscr{L} \text{ such that } (w, \ell) \in \mathscr{B}_{\text{extended}} \}.$ 

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as a projection:

► as solutions of equations: kernel representation  $f: \mathscr{U} \to \bullet, \qquad \mathscr{B} = \{w \in \mathscr{U} \mid f(w) = 0\},$ 

latent variable representation

 $\mathscr{B} = \{ w \in \mathscr{U} \mid \exists \ \ell \in \mathscr{L} \text{ such that } (w, \ell) \in \mathscr{B}_{\text{extended}} \},\$ 

*w*'s 'manifest' variables: the variables the model aims at,  $\ell$ 's 'latent' variables: auxiliary variables.


#### latent variable representation

 $\mathscr{B} = \{ w \in \mathscr{U} \mid \exists \ \ell \in \mathscr{L} \text{ such that } (w, \ell) \in \mathscr{B}_{\text{extended}} \},\$ 



## The elimination theorem

Assume that the (equations specifying the) extended behavior  $\mathscr{B}_{extended}$  has a certain structure.

**Does the manifest behavior**  $\mathcal{B}$  **retain this structure?** 

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**'Structure':** linearity, open, closed, (semi-)algebraic variety, polyhedron, solution set of ODEs, behavior of LTIDS, ...

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We have illustrated the emergence of latent variables, and their elimination in a few examples.

### Examples

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 $\mathcal{B}_{extended} \text{ linear} \Rightarrow \mathscr{B} \text{ linear.} \\ \mathscr{B}_{extended} \text{ time-invariant} \Rightarrow \mathscr{B} \text{ time-invariant.}$ 

## Examples

- $\begin{array}{ll} & & & & \\ & & & & \\ & & & \\ & & & & \\ & & & \\ & & &$
- $\blacktriangleright \mathscr{B}_{extended} \text{ differential} \Rightarrow \mathscr{B} \text{ differential }?$ 
  - $\mathscr{B}_{\text{extended}}$  **LTIDS**  $\Rightarrow \mathscr{B}$  **LTIDS**?



Consider the dynamical system  $\Sigma = (\mathbb{T}, \mathbb{W}_1 \times \mathbb{W}_2, \mathscr{B}).$ 

**Define the projection**  $\Sigma_1 = (\mathbb{T}, \mathbb{W}_1, \mathscr{B}_1)$  with

 $\mathscr{B}_1 = \{w_1 : \mathbb{T} \to \mathbb{W}_1 \mid \exists w_2 : \mathbb{T} \to \mathbb{W}_2 \text{ such that } (w_1, w_2) \in \mathscr{B} \}.$ 

In the LTIDS case,  $\mathscr{B} \in \mathscr{L}^{w_1+w_2}$ ,  $\mathscr{B} \subseteq \mathscr{C}^{\infty}(\mathbb{R}, \mathbb{R}^{w_1+w_2})$ . Therefore,  $\mathscr{B}_1 \subseteq \mathscr{C}^{\infty}(\mathbb{R}, \mathbb{R}^{w_1})$ .



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In the LTIDS case,  $\mathscr{B} \in \mathscr{L}^{\mathsf{w}_1 + \mathsf{w}_2}$ ,  $\mathscr{B} \subseteq \mathscr{C}^{\infty}(\mathbb{R}, \mathbb{R}^{\mathsf{w}_1 + \mathsf{w}_2})$ . Therefore,  $\mathscr{B}_1 \subseteq \mathscr{C}^{\infty}(\mathbb{R}, \mathbb{R}^{\mathsf{w}_1})$ .

The question which we consider is if, when  $\Sigma$  is a LTIDS,  $\Sigma_1$  is also a LTIDS. In other words,

$$\llbracket \mathscr{B} \in \mathscr{L}^{\mathsf{w}_1 + \mathsf{w}_2} \rrbracket \Rightarrow \llbracket \mathscr{B}_1 \in \mathscr{L}^{\mathsf{w}_1} \rrbracket ?$$

### In a picture



$$\llbracket \mathscr{B} \in \mathscr{L}^{\mathsf{w}_1 + \mathsf{w}_2} \rrbracket \Rightarrow \llbracket \mathscr{B}_1 \in \mathscr{L}^{\mathsf{w}_1} \rrbracket ?$$

**Elimination theorem** 



**Elimination theorem** 

#### **Theorem**

#### $\mathscr{L}^{\bullet}$ is closed under projection, that is,

$$\llbracket \mathscr{B} \in \mathscr{L}^{\mathsf{w}_1 + \mathsf{w}_2} \rrbracket \Rightarrow \llbracket \mathscr{B}_1 \in \mathscr{L}^{\mathsf{w}_1} \rrbracket$$

With

$$R_1\left(\frac{d}{dt}\right)w_1 = R_2\left(\frac{d}{dt}\right)w_2$$

a kernel representation of  $\mathcal{B}$ , and

$$R\left(\frac{d}{dt}\right)w_1 = 0$$

a kernel representation of  $\mathscr{B}_1$ , we think of this theorem as *'elimination'* of the variables  $w_2$  from the equations.

- Let  $R_1\left(\frac{d}{dt}\right)w_1 = R_2\left(\frac{d}{dt}\right)w_2$  be a kernel representation of  $\mathscr{B}$ .
- Note that it can be assumed, without loss of generality, that R<sub>2</sub> is in Smith form,

$$R_2 = \begin{bmatrix} R'_2 \\ R''_2 \end{bmatrix} = \begin{bmatrix} \mathtt{diag}(d_1, d_2, \dots, d_r) & \mathbf{0}_{r \times (n_2 - r)} \\ \mathbf{0}_{(n_1 - r) \times r} & \mathbf{0}_{(n_1 - r) \times (n_2 - r)} \end{bmatrix},$$

with  $d_1, d_2, ..., d_r \neq 0$ .

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**Observe that**  $R'_2\left(\frac{d}{dt}\right)$  is a surjective operator (see **Proposition 4 of the section on differential operators).** 

- Let  $R_1\left(\frac{d}{dt}\right)w_1 = R_2\left(\frac{d}{dt}\right)w_2$  be a kernel representation of  $\mathscr{B}$ .
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with  $d_1, d_2, ..., d_r \neq 0$ .

**Observe that**  $R'_2\left(\frac{d}{dt}\right)$  is a surjective operator (see **Proposition 4 of the section on differential operators**).

• **Partition** 
$$R_1 = \begin{bmatrix} R'_1 \\ R''_1 \end{bmatrix}$$
 **conformably to**  $R_2 = \begin{bmatrix} R'_2 \\ R''_2 \end{bmatrix}$ .  
**Then**  $R''_1 \left(\frac{d}{dt}\right) w_1 = 0$  is a kernel representation of  $\mathscr{B}_1$ .

Elimination of state variables (x) in input/state/output systems:

$$\frac{d}{dt}x = Ax + Bu, y = Cx + Du, \quad \rightsquigarrow \quad P\left(\frac{d}{dt}\right)y = Q\left(\frac{d}{dt}\right)u.$$

Elimination of nuisance variables (x) in DAEs:

$$E\frac{d}{dt}x = Ax + Bw \quad \rightsquigarrow \quad R\left(\frac{d}{dt}\right)w = 0.$$

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**Elimination of latent variables (** $\ell$ **):** 

$$R\left(\frac{d}{dt}\right)w = M\left(\frac{d}{dt}\right)\ell \quad \rightsquigarrow \quad R'\left(\frac{d}{dt}\right)w = 0.$$

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**Elimination of latent variables**  $(\ell)$ **:** 

$$R\left(\frac{d}{dt}\right)w = M\left(\frac{d}{dt}\right)\ell \quad \rightsquigarrow \quad R'\left(\frac{d}{dt}\right)w = 0.$$

 $\blacktriangleright$   $\mathscr{L}^{\bullet}$  is closed under

intersection, addition (see Exercise III.3), and projection.

For the RLC circuit, KCL, the constitutive equations, and the manifest variable assignment: all linear constant-coefficient differential equations — most of them algebraic equations (zero-th order), but linear constant-coefficient differential equations nevertheless.

Elimination theorem  $\Rightarrow$  the latent variables (the potentials of the vertices and the currents in the edges) can be completely eliminated.  $\Rightarrow$  the port behavior is described by linear constant-coefficient differential equations.

Since there are 2 real port variables, there could be 0, 1, or 2 differential equations that govern the port behavior. We derived that the behavior is described by *one* the differential equation. To prove that there is **exactly one** for a minimal kernel representation for the port behavior requires use of the passivity properties of the circuit elements.

# **Elimination algorithm**



Start with  $(R_1, R_2) \in \mathbb{R}[\xi]^{\bullet \times \bullet}$ , parametrizing the LTIDS  $R_1\left(\frac{d}{dt}\right)w_1 = R_2\left(\frac{d}{dt}\right)w_2$ . <u>Problem</u>: compute  $R'_1 \in \mathbb{R}[\xi]^{\bullet \times \bullet}$ , parametrizing the projected LTIDS  $R'_1\left(\frac{d}{dt}\right)w_1 = 0$ , with  $w_2$  eliminated. Algorithm

Start with  $(R_1, R_2) \in \mathbb{R}[\xi]^{\bullet \times \bullet}$ ,

<u>**Problem:**</u> compute  $R'_1 \in \mathbb{R}[\xi]^{\bullet \times \bullet}$ ,



$$\left\{f\in\mathbb{R}\left[\xi
ight]^{1 imes ext{rowdimension}(R_{2})}\mid fR_{2}=0
ight\}$$

is called the *left syzygy* of  $R_2$ . It is obviously an  $\mathbb{R}[\xi]$ -module.

Compute a basis for the left syzygy of  $R_2$ . Let F be a matrix whose rows form a basis for this syzygy. Computing such a basis is a standard problem in computer algebra.



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<u>**Problem:**</u> compute  $R'_1 \in \mathbb{R}[\xi]^{\bullet \times \bullet}$ ,

Compute a basis for the left syzygy of R<sub>2</sub>. Let F be a matrix whose rows form a basis for this syzygy.
 Computing such a basis is a standard problem in computer algebra.

$$\blacktriangleright \quad R_1' = FR_1.$$

# **Modeling RLC circuits**

# **Notions from graph theory**



A graph is one of the most useful notions from mathematics, with applications in almost every applied area.

It is instructive to think of a graph as a set of points, called vertices, and lines, called edges, connecting pairs of points.



The formal definition is a follows.



### A graph *G* is defined as

$$\mathscr{G} = (\mathbb{V}, \mathbb{E}, f)$$

with  $\mathbb{V}$  the finite set of vertices,  $\mathbb{E}$  the finite set of edges, *f* the incidence map;

*f* maps each element  $e \in \mathbb{E}$  into an <u>unordered</u> pair  $f(e) = [v_1, v_2]$  with  $v_1, v_2 \in \mathbb{V}$ .

If  $f(e) = [v_1, v_2]$ , then we call  $v_1$  and  $v_2$  *incident* to  $e \in \mathbb{E}$ .

**<u>Notation</u>:**  $\{a,b\} =$  the set with elements a and b;  $\{a,b\} = \{b,a\}$  and, if a = b,  $\{a,b\} = \{a\}$ . (a,b) = the ordered pair of elements a and b;  $(a,b) \neq (b,a)$  unless a = b. [a,b] = the unordered pair of elements a,b; [a,b] = [b,a].





$$\mathbb{V} = \{v_1, v_2, v_3, v_4\}, \\ \mathbb{E} = \{e_1, e_2, e_3, e_4\}, \\ f : e_1 \mapsto [v_1, v_2], e_2 \mapsto [v_1, v_3], e_3 \mapsto [v_2, v_4], e_4 \mapsto [v_3, v_4].$$

The edge *e* is called a *self-loop* if f(e) = [v, v].

A convenient way of specifying a graph without self-loops in mathematical notation is by its **incidence matrix.** 

The incidence matrix is a matrix of 0's and 1's having |V| rows and |E| columns, with (k, ℓ)-th element = 1 if the ℓ-th edge is incident to the k-th vertex, = 0 otherwise.

**<u>Notation</u>**: |S| = the *cardinality* of the set S. If S is finite, then the cardinality = the number of elements. A convenient way of specifying a graph without self-loops in mathematical notation is by its **incidence matrix.** 

The incidence matrix is a matrix of 0's and 1's having |V| rows and |E| columns, with (k, ℓ)-th element = 1 if the ℓ-th edge is incident to the k-th vertex, = 0 otherwise.

For our example, the incidence matrix equals

$$\begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$



A directed graph is a graph in which each edge is assigned a direction. Think of a digraph as a set of points and lines with arrows pointing from one edge to another.



The formal definition is as follows.



### A directed graph, or digraph, *G* is defined as

 $\mathscr{G} = (\mathbb{V}, \mathbb{E}, f)$ 

with  $\mathbb{V}$  the finite set of vertices,  $\mathbb{E}$  the finite set of edges, f the incidence map; f maps each element  $e \in \mathbb{E}$  into

an <u>ordered</u> pair  $f(e) = (v_1, v_2)$  with  $v_1, v_2 \in \mathbb{V}$ .

If  $f(e) = (v_1, v_2)$ , then we call  $v_1$  and  $v_2$  *incident* to  $e \in \mathbb{E}$ .  $v_1$  is the *source* of e and  $v_2$  is the *sink* of e. We think of e as being directed from  $v_1$  to  $v_2$ .

The edge *e* is called a *self-loop* if f(e) = (v, v).





$$\mathbb{V} = \{v_1, v_2, v_3, v_4\}, \\ \mathbb{E} = \{e_1, e_2, e_3, e_4\}, \\ f : e_1 \mapsto (v_1, v_2), e_2 \mapsto (v_1, v_3), e_3 \mapsto (v_2, v_4), e_4 \mapsto (v_3, v_4).$$

A convenient way of specifying a digraph without self-loops is by its **incidence matrix.** 

The incidence matrix is a matrix of 0's, +1's, and -1's having |V| rows and |E| columns, with  $(k, \ell)$ -th element

- = +1 if the k-th vertex is the source for the  $\ell$ -th edge,
- = -1 if the k-th vertex is the sink for the  $\ell$ -th edge,
- = 0 otherwise.

**Caveat**:

Sometimes the opposite convention for +1 and -1 is used!

A convenient way of specifying a digraph without self-loops is by its **incidence matrix.** 

The incidence matrix is a matrix of 0's, +1's, and −1's having |V| rows and |E| columns, with (k, ℓ)-th element = +1 if the k-th vertex is the source for the ℓ-th edge,

- = -1 if the k-th vertex is the sink for the  $\ell$ -th edge,
- = 0 otherwise.

For our example, the incidence matrix equals

$$\begin{bmatrix} +1 & +1 & 0 & 0 \\ -1 & 0 & +1 & 0 \\ 0 & -1 & 0 & +1 \\ 0 & 0 & -1 & -1 \end{bmatrix}$$
Graph with leaves

A graph with leaves is like an ordinary graph except that some of the edges are incident to only one vertex. Think of a graph with leaves as a set of points, called vertices, lines, called edges, connecting pairs of points, and leaves, that connect to one point only.



The formal definition is a follows.

### A graph with leaves $\mathscr{G}$ is defined as

$$\mathscr{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, f_{\mathbb{E}}, f_{\mathbb{L}})$$

with  $\mathbb{V}, \mathbb{E}$ , and  $f_{\mathbb{E}}$ , the edge incidence map, defined as for graphs,  $\mathbb{L}$  the finite set of edges,

 $f_{\mathbb{L}}$ , the edge incidence map, maps each element  $\ell \in \mathbb{L}$  into an element  $f_{\mathbb{L}}(\ell) \in \mathbb{V}$ .

If  $f_{\mathbb{L}}(\ell) = v$ , then we call  $\ell \in \mathbb{L}$  *incident* to  $e \in \mathbb{E}$ .





$$\mathbb{V} = \{ v_1, v_2, v_3, v_4 \}, \mathbb{E} = \{ e_1, e_2, e_3, e_4 \}, \mathbb{L} = \{ \ell_1, \ell_2 \}, \\ f_{\mathbb{E}} : e_1 \mapsto (v_1, v_2), e_2 \mapsto (v_1, v_3), e_3 \mapsto (v_2, v_4), e_4 \mapsto (v_3, v_4), \\ f_{\mathbb{L}} : \ell_1 \mapsto v_1, \ell_2 \mapsto v_4.$$

A convenient way of specifying a graph with leaves without self-loops is by its **incidence matrices.** 

The edge incidence matrix  $\mathbb{A}_{\mathbb{E}}$  is defined as for graphs, the leaf incidence matrix  $\mathbb{A}_{\mathbb{L}}$  is a matrix of 0's and 1's having  $|\mathbb{V}|$  rows and  $|\mathbb{L}|$  columns, with  $(k, \ell)$ -th element = 1 if the  $\ell$ -th leaf is incident to the k-th vertex, = 0 otherwise. A convenient way of specifying a graph with leaves without self-loops is by its **incidence matrices.** 

The edge incidence matrix  $\mathbb{A}_{\mathbb{E}}$  is defined as for graphs, the leaf incidence matrix  $\mathbb{A}_{\mathbb{L}}$  is a matrix of 0's and 1's having  $|\mathbb{V}|$  rows and  $|\mathbb{L}|$  columns, with  $(\mathbb{k}, \ell)$ -th element = 1 if the  $\ell$ -th leaf is incident to the k-th vertex, = 0 otherwise.

For our example, the incidence matrices equal

$$\mathbb{A}_{\mathbb{E}} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix}, \quad \mathbb{A}_{\mathbb{L}} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix}$$

**Digraph with leaves** 

A digraph with leaves is like an ordinary graph with leaves except that each edge and leaf is assigned a direction.



The formal definition is a follows.

### A digraph with leaves $\mathscr{G}$ is defined as

$$\mathscr{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, f_{\mathbb{E}}, f_{\mathbb{L}})$$

with  $\mathbb{V}, \mathbb{E}$ , and  $f_{\mathbb{E}}$ , the edge incidence map, defined as for graphs,

 $f_{\mathbb{L}}$ , the edge incidence map, maps each element  $\ell \in \mathbb{L}$  into an element  $f_{\mathbb{L}}(\ell) \in \mathbb{V}$ , and assigns to each leaf  $\ell$  a direction, either away from the vertex  $f_{\mathbb{L}}(\ell)$ , in which case the vertex is called the *source* of  $\ell$ , or into the vertex  $f_{\mathbb{L}}(\ell)$ , in which case the vertex is the vertex is called the *sink* of  $\ell$ .





 $\mathbb{V} = \{v_1, v_2, v_3, v_4\}, \mathbb{E} = \{e_1, e_2, e_3, e_4\}, \mathbb{L} = \{\ell_1, \ell_2\}, \\ f_{\mathbb{E}} : e_1 \mapsto (v_1, v_2), e_2 \mapsto (v_1, v_3), e_3 \mapsto (v_2, v_4), e_4 \mapsto (v_3, v_4), \\ f_{\mathbb{L}} : \ell_1 \mapsto v_1 \text{ (sink)}, \ell_2 \mapsto v_4 \text{ (sink)}.$ 

A convenient way of specifying a digraph with leaves without self-loops is by its **incidence matrices.** 

- The edge incidence matrix  $\mathbb{A}_{\mathbb{E}}$  is defined as for digraphs,
- the leaf incidence matrix  $\mathbb{A}_{\mathbb{L}}$  is a matrix of 0's, +1's, and
- $-1\text{'s, having} \ |\mathbb{V}| \ \text{rows and} \ |\mathbb{L}| \ \text{columns, with} \ (\mathtt{k},\ell)\text{-th element}$ 
  - = +1 if the  $\ell$ -th leaf is incident to the k-th vertex, a source,
  - = -1 if the  $\ell$ -th leaf is incident to the k-th vertex, a sink,
  - = 0 otherwise.

A convenient way of specifying a digraph with leaves without self-loops is by its **incidence matrices.** 

- The edge incidence matrix  $\mathbb{A}_{\mathbb{E}}$  is defined as for digraphs,
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  - = +1 if the  $\ell$ -th leaf is incident to the k-th vertex, a source,
  - = -1 if the  $\ell$ -th leaf is incident to the k-th vertex, a sink,
  - = 0 otherwise.

#### For our example, the incidence matrices equal

$$\mathbb{A}_{\mathbb{E}} = \begin{bmatrix} +1 & +1 & 0 & 0 \\ -1 & 0 & +1 & 0 \\ 0 & -1 & 0 & +1 \\ 0 & 0 & -1 & -1 \end{bmatrix}, \quad \mathbb{A}_{\mathbb{L}} = \begin{bmatrix} -1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1 \end{bmatrix}$$

## The interaction variables



We view an electrical as a device, with a finite number of wires, called *terminals*, sticking out of it. The electrical circuit interacts with its environment through these terminals.



Modeling the electrical circuit means coming up with a specification of this interaction.



We view an electrical as a device, with a finite number of wires, called *terminals*, sticking out of it. The electrical circuit interacts with its environment through these terminals.



Modeling the electrical circuit means coming up with a specification of this interaction.

How do we describe this interaction? What are the interaction variables?

#### **Voltages and currents**



The natural choice is to take for the interaction variables

- the currents into the circuit along the terminals,
- **•** the voltages across the terminals.

#### **Voltages and currents**



#### This leads to the following terminal variables

 $I_1, I_2, \ldots, I_N,$ 

 $V_{1,1}, V_{1,2}, \ldots, V_{1,N}, V_{2,1}, V_{2,2}, \ldots, V_{2,N}, \ldots, V_{N,1}, V_{N,2}, \ldots, V_{N,N},$ 

with  $I_k$  = the current flowing into the circuit along terminal k,  $V_{k_1,k_2}$  = the voltage between terminal  $k_1$  and  $k_2$ .

#### **Voltages and currents**



#### As sign convention we take

 $I_k > 0$  if along terminal k the current flows into the circuit,  $V_{k_1,k_2} > 0$  if the voltage drop from terminal  $k_1$  to  $k_2$  is positive. The voltage/current behavior

**Organizing these variables as vectors and matrices leads to** 

$$I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix}, \quad V = \begin{bmatrix} V_{1,1} & V_{1,2} & \cdots & V_{1,N} \\ V_{2,1} & V_{2,2} & \cdots & V_{2,N} \\ \vdots & \vdots & \cdots & \vdots \\ V_{N,1} & V_{N,2} & \cdots & V_{N,N} \end{bmatrix}$$

→ the dynamical system  $\Sigma = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^{N \times N}, \mathscr{B}_{IV}).$  $(I,V) \in \mathscr{B}_{IV}$  means that the trajectory of currents and voltages  $(I,V) : \mathbb{R} \to \mathbb{R}^N \times \mathbb{R}^{N \times N}$  is compatible with the circuit architecture and its element values. The aim of circuit modeling is to specify  $\mathscr{B}_{IV}$ .

The subscript in  $\mathscr{B}_{IV}$  refers to the choice of currents and voltages as the variables that describe the interaction. We will see other choices of terminal variables soon.

**Kirchhoff's laws** 

The behavior  $\mathscr{B}_{IV}$  is said to satisfy Kirchhoff's current law (KCL) if

$$\llbracket (I,V) \in \mathscr{B}_{IV} \rrbracket \Rightarrow \llbracket I_1 + I_2 + \dots + I_N = 0 \rrbracket,$$



Gustav Kirchhoff (1824-1887)

#### and Kirchhoff's voltage law (KVL) if

$$\llbracket (I,V) \in \mathscr{B}_{IV} \text{ and } \Bbbk_1, \Bbbk_2, \dots, \Bbbk_n \in \{1,2,\dots,N\} \rrbracket$$
$$\Rightarrow \llbracket V_{\Bbbk_1, \Bbbk_2} + V_{\Bbbk_2, \Bbbk_3} + \dots + V_{\Bbbk_{n-1}, \Bbbk_n} + V_{\Bbbk_n, \Bbbk_1} = 0 \rrbracket.$$

KCL means that the circuit stores no net charge, while KVL means that the sum of the voltage drops across a cycle is zero.



Let  $\mathscr{K} \subset \mathbb{R}^{N \times N}$  and  $\underline{e} \in \mathbb{R}^N$  be defined as follows

$$\mathscr{K} = \{ M \in \mathbb{R}^{N \times N} \mid M_{k_1, k_2} + M_{k_2, k_3} + \dots + M_{k_{n-1}, k_n} + M_{k_n, k_1} = 0$$
  
for all  $k_1, k_2, \dots, k_n \in \{1, 2, \dots, N\} \},$ 





**Proposition: Define the map**  $L : \mathbb{R}^N \to \mathbb{R}^{N \times N}$  by

$$L: P \mapsto Pe^{\top} - eP^{\top}$$

**There holds** 

 $image(L) = \mathscr{K}$  and kernel(L) = span(e).

This proposition implies that for each  $M \in \mathcal{K}$ , there exists  $P \in \mathbb{R}^{\mathbb{N}}$  such that

$$M = Pe^{\top} - eP^{\top}, \quad \text{i.e., } M_{k,\ell} = P_k - P_\ell$$



Assume that  $\mathscr{B}_{IV}$  satisfies KVL. Then we can express  $V(t) : \mathbb{R} \to \mathbb{R}^{N \times N}$  as  $V(t) = P(t)e^{\top} - eP(t)^{\top}$  for some  $P : \mathbb{R} \to \mathbb{R}^N$ . Call  $P_k$  the potential of terminak k. The voltages are related to the potentials by

$$V_{\mathbf{k}_1,\mathbf{k}_2} = P_{\mathbf{k}_1} - P_{\mathbf{k}_2}.$$



It follows that (assuming KVL) we can take for the interaction variables

- **b** the **currents** into the circuit along the terminals,
- **b** the **potentials** of the terminals.

This leads to the dynamical system  $\Sigma = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B})$ .  $(I, P) \in \mathscr{B}_{IV}$  means that the trajectory of currents and potentials  $(I, P) : \mathbb{R} \to \mathbb{R}^N \times \mathbb{R}^N$  is compatible with the circuit architecture and its element values. The aim of circuit modeling is to specify  $\mathscr{B}$ . **Electrical circuit** 

Summarizing, we arrive at the following alternative definition of a circuit behavior. We use this definition in the sequel.



#### At each terminal:

a **potential (!)** and a **current** (counted > 0 into the circuit),

**Electrical circuit** 

Summarizing, we arrive at the following alternative definition of a circuit behavior. We use this definition in the sequel.



#### At each terminal:

a **potential (!)** and a **current** (counted > 0 into the circuit),

 $\rightsquigarrow$  behavior  $\mathscr{B} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$ .

 $(V_1, V_2, \ldots, V_N, I_1, I_2, \ldots, I_N) \in \mathscr{B}$  means: this potential/current trajectory is compatible with the circuit architecture and its element values.

#### Kirchhoff's laws

Kirchhoff's laws now take the following form. The behavior *B* satisfies Kirchhoff's current law (KCL) if

$$\llbracket (I,P) \in \mathscr{B} \rrbracket \Rightarrow \llbracket I_1 + I_2 + \dots + I_N = 0 \rrbracket,$$



Gustav Kirchhoff (1824-1887)

and Kirchhoff's voltage law (KVL) if

$$\llbracket (I,P) \in \mathscr{B} \text{ and } \alpha : \mathbb{R} \to \mathbb{R} \rrbracket \Rightarrow \llbracket (I,P+\alpha e) \in \mathscr{B} \rrbracket.$$

KCL means that the circuit stores no net charge, while KVL means that the potentials are defined only up to an additive constant (that may change in time).

## **Circuit specification**

We now explain how one can formally describe a circuit.

Some of the aspects of our formalization take into account that we are only interested in describing linear passive RLC circuits. The ideas are applicable to more general situations, but some details have to be adapted. We now explain how one can formally describe a circuit.

An RLC circuit is defined through its architecture, a digraph with leaves,

$$\mathscr{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, f_{\mathbb{E}}, f_{\mathbb{L}}).$$

Assume that the leaves are all sinks, in the sense that they are incident towards a vertex.

The circuit elements (R's, L's, and C's) are imbedded in the edges, the vertices correspond to connectors, and the leaves correspond to the terminals by which the circuit interacts with its environment.

We now explain how one can formally describe a circuit.

An RLC circuit is defined through its architecture, a digraph with leaves,

$$\mathscr{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, f_{\mathbb{E}}, f_{\mathbb{L}}).$$

Assume that the leaves are all sinks, in the sense that they are incident towards a vertex.

and its element specification. This assigns to each vertex, either a resistance value  $R \ge 0$ , or an inductance value L > 0, or a capacitance value C > 0.



#### For the 2-terminal circuit





#### For the 2-terminal circuit, the circuit architecture is





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and the element specification is

- $e_1 \mapsto$  resistance  $R_C$ ,  $e_2 \mapsto$  inductance L,  $e_3 \mapsto$  capacitance C,
- $e_4 \mapsto$  resistance  $R_L$ .

# **Circuit equations**

### **Obtain 4 matrices from the circuit description:**

- $\blacktriangleright \quad \mathbb{A}_{\mathbb{E}}, \text{ the edge incidence matrix, a } |\mathbb{V}| \times |\mathbb{E}| \text{ matrix having values } +1, \\ -1, \text{ and } 0,$
- $\blacktriangleright \quad \mathbb{A}_{\mathbb{L}}, \text{ the leaf incidence matrix, a } |\mathbb{V}| \times |\mathbb{L}| \text{ matrix, having values } +1 \text{ and } 0,$
- $Z, \text{ the impedance matrix, a } |\mathbb{E}| \times |\mathbb{E}| \text{ diagonal polynomial matrix with} \\ Z(\xi)_{k,k} = \begin{cases} R_k \text{ if a resistor with value } R_k \text{ is in edge } e_k, \\ L_k \xi \text{ if an inductor with value } L_k \text{ is in edge } e_k, \\ 1 \text{ otherwise}, \end{cases}$
- > *Y*, the admittance matrix, a  $|\mathbb{E}| \times |\mathbb{E}|$  diagonal polynomial matrix with

$$Y(\xi)_{k,k} = \begin{cases} C_k \xi \text{ if an capacitor with value } C_k \text{ is in edge } e_k, \\ 1 \text{ otherwise.} \end{cases}$$

**Mathematical circuit specification** 

From these 4 matrices, we obtain directly the circuit equations. These involve as manifest variables, the terminal currents and potentials



and as latent variables, the edge currents, the edge voltages, and the vertex potentials





#### The circuit equations are

$$V_{\mathbb{E}} = \mathbb{A}_{\mathbb{E}}^{\top} P_{\mathbb{V}},$$
$$Z\left(\frac{d}{dt}\right) I_{\mathbb{E}} = Y\left(\frac{d}{dt}\right) V_{\mathbb{E}},$$
$$\mathbb{A}_{\mathbb{E}} I_{\mathbb{E}} + \mathbb{A}_{\mathbb{L}} I = 0,$$
$$\mathbb{A}_{\mathbb{L}}^{\top} P_{\mathbb{V}} + P = 0.$$


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 $\mathbb{A}_{\mathbb{E}} I_{\mathbb{E}} + \mathbb{A}_{\mathbb{L}} I = 0,$   
 $\mathbb{A}_{\mathbb{L}}^{\top} P_{\mathbb{V}} + P = 0.$ 

The variables  $V_{\mathbb{E}}$  can be eliminated immediately, leading to the 'modified nodal analysis' circuit equations

$$Z\left(\frac{d}{dt}\right)I_{\mathbb{E}} = Y\left(\frac{d}{dt}\right)\mathbb{A}_{\mathbb{E}}^{\top}P_{\mathbb{V}}, \mathbb{A}_{\mathbb{E}}I_{\mathbb{E}} + \mathbb{A}_{\mathbb{L}}I = 0, \mathbb{A}_{\mathbb{L}}^{\top}P_{\mathbb{V}} + P = 0,$$

with (I, P) as manifest and  $(I_{\mathbb{E}}, P_{\mathbb{V}})$  as latent variables.



## Equation

$$V_{\mathbb{E}} = \mathbb{A}_{\mathbb{E}}^{\top} P_{\mathbb{V}}$$

relates the vertex potentials to the voltages across the edges;

$$Z\left(\frac{d}{dt}\right)I_{\mathbb{E}} = Y\left(\frac{d}{dt}\right)V_{\mathbb{E}}$$

expresses the constitutive laws of the resistors, inductors, and capacitors in the edges;

$$\mathbb{A}_{\mathbb{E}}I_{\mathbb{E}} + \mathbb{A}_{\mathbb{L}}I = 0$$

is KCL for each of the vertices; and

$$\mathbb{A}_{\mathbb{L}}^{\top} P_{\mathbb{V}} + P = 0$$

assigns the terminal potentials to the corresponding vertex potentials.













### Leading to the MNA equations

$$\begin{aligned} R_{C}I_{e_{1}} &= P_{v_{1}} - P_{v_{2}}, \quad L\frac{d}{dt}I_{e_{2}} = P_{v_{1}} - P_{v_{3}}, \\ I_{e_{1}} &= C\frac{d}{dt}\left(P_{v_{2}} - P_{v_{4}}\right), \quad R_{L}I_{e_{4}} = P_{v_{3}} - P_{v_{4}}; \\ I_{1} &= I_{e_{1}} + I_{e_{2}}, \quad I_{e_{2}} = I_{e_{3}}, \quad I_{e_{4}} = I_{e_{4}}, \quad I_{2} = I_{e_{1}} + I_{e_{2}}; \\ P_{1} &= P_{e_{1}}, \quad P_{2} = P_{e_{4}}. \end{aligned}$$



#### Leading to the MNA equations

$$\begin{aligned} R_{C}I_{e_{1}} &= P_{v_{1}} - P_{v_{2}}, \quad L\frac{d}{dt}I_{e_{2}} = P_{v_{1}} - P_{v_{3}}, \\ I_{e_{1}} &= C\frac{d}{dt}\left(P_{v_{2}} - P_{v_{4}}\right), \quad R_{L}I_{e_{4}} = P_{v_{3}} - P_{v_{4}}; \\ I_{1} &= I_{e_{1}} + I_{e_{2}}, \quad I_{e_{2}} = I_{e_{3}}, \quad I_{e_{4}} = I_{e_{4}}, \quad I_{2} = I_{e_{1}} + I_{e_{2}}; \\ P_{1} &= P_{e_{1}}, \quad P_{2} = P_{e_{4}}. \end{aligned}$$

The MNA circuit equations can be set up in a straightforward way. The manifest variables are the terminal currents and potentials. MNA illustrates the systematic way in which equations can be set up from first principles, with as choice of latent variables are the vertex potentials and edge currents.

# Recapitulation



- First principles models invariably contain latent variables.
- It may or may not be possible to eliminate the latent variables.



- First principles models invariably contain latent variables.
- It may or may not be possible to eliminate the latent variables.
- The behavior of LTIDSs is closed under projection. In LTIDSs latent variables can be completely eliminated.
- Elimination algorithms involve computing a set of generators of a left syzygy.



- First principles models invariably contain latent variables.
- It may or may not be possible to eliminate the latent variables.
- The behavior of LTIDSs is closed under projection. In LTIDSs latent variables can be completely eliminated.
- Elimination algorithms involve computing a set of generators of a left syzygy.
- > The modeling of the terminal behavior of general RLC circuits can be done by MNA.
- A crucial step in this modeling procedure is the choice of latent variables.

# **End of Lecture IV**