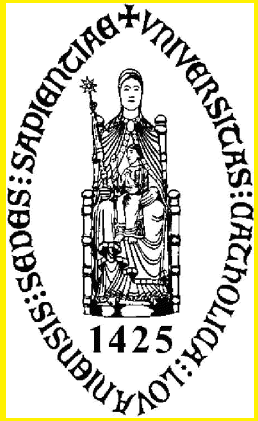

A POST MODERN VIEW

of some of the basics of

ELECTRICAL CIRCUIT THEORY

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K.U. Leuven

Workshop Mathematical Aspects of Network Synthesis **Würzburg, September 28, 2010**

Aim

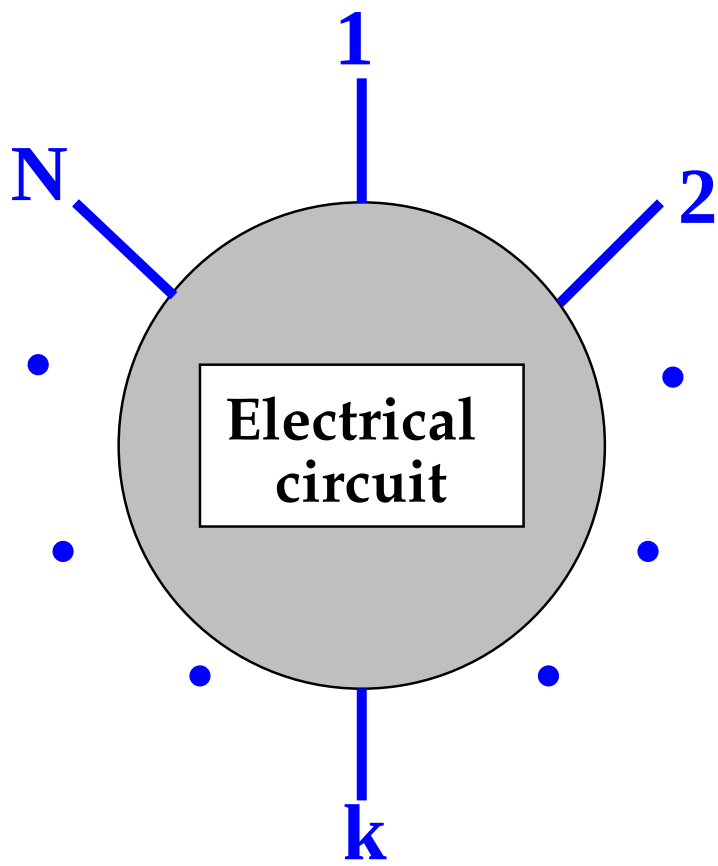
To present an approach to mathematizing a (simple) part of physics:

electrical circuits.

I feel that I finally understand circuits, after all this time.

Electrical circuit

wires $\cong$ ‘terminals’

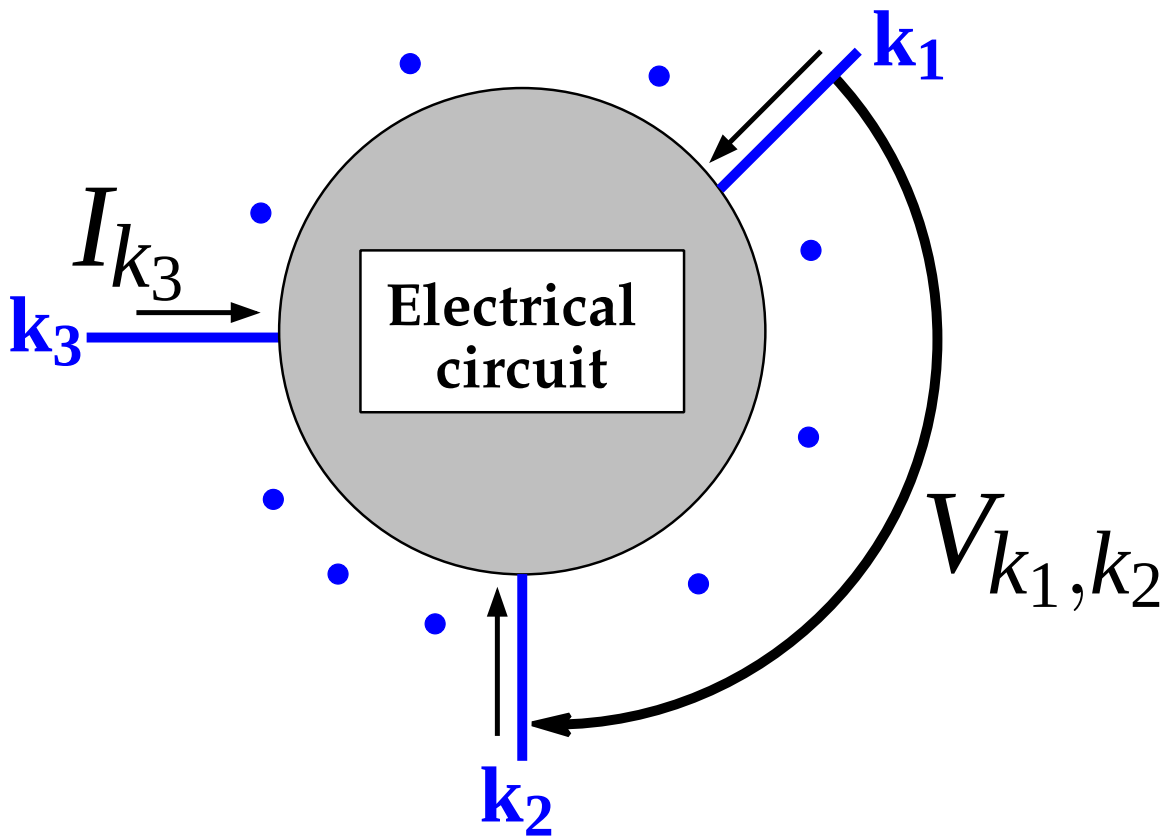


¡¡ Describe electrical interaction with environment !!

By what physically measurable variables does the circuit interacts with its environment?

Interaction variables

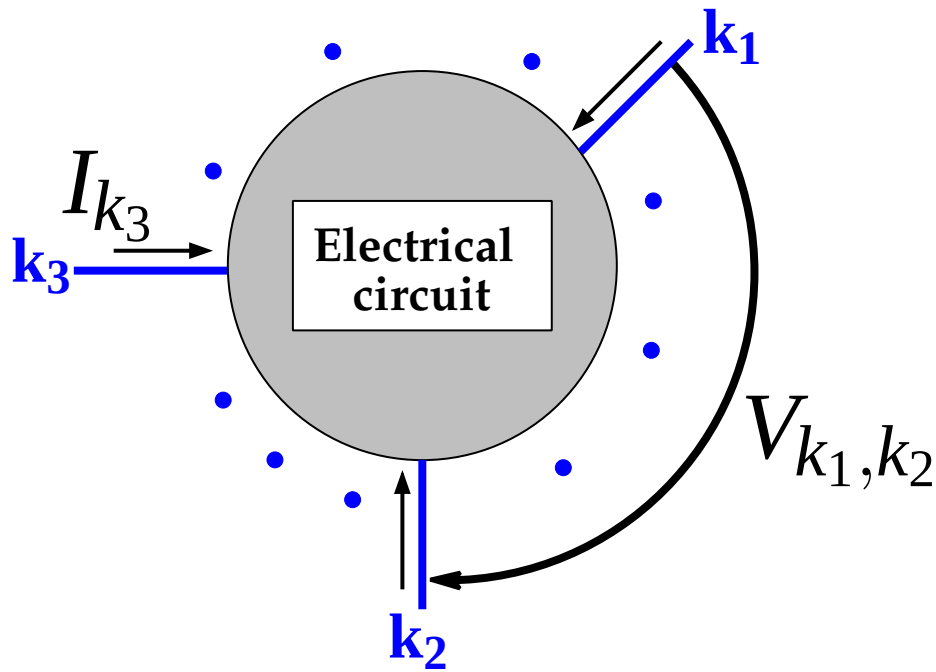
Interaction variables



<u>interaction variables</u>: currents in & voltages across.

measurable by ammeters and voltmeters.

Currents and voltages



$$\rightsquigarrow \qquad I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix}, \quad V = \begin{bmatrix} V_{1,1} & V_{1,2} & \cdots & V_{1,N} \\ V_{2,1} & V_{2,2} & \cdots & V_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ V_{N,1} & V_{N,2} & \cdots & V_{N,N} \end{bmatrix}.$$

Currents and voltages

$$\rightsquigarrow \qquad I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix}, \quad V = \begin{bmatrix} V_{1,1} & V_{1,2} & \cdots & V_{1,N} \\ V_{2,1} & V_{2,2} & \cdots & V_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ V_{N,1} & V_{N,2} & \cdots & V_{N,N} \end{bmatrix}.$$

$$\rightsquigarrow \Sigma_{IV} = \left(\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^{N\times N}, \mathscr{B}_{IV}\right), \quad \mathscr{B}_{IV} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^{N\times N}\right)^{\mathbb{R}}.$$

$(I,V) \in \mathscr{B}_{IV}$ **means**

$$\left(I_1, I_2, \ldots, I_k, \ldots, I_N, V_{1,1}, V_{1,2}, \ldots, V_{k_1,k_2}, \ldots, V_{N,N}\right) : \mathbb{R} \longrightarrow \mathbb{R}^N \times \mathbb{R}^{N\times N}$$

is compatible with the circuit architecture and its element values. I.e., all the trajectories that can conceivable occur.

Kirchhoff voltage law (KVL):

$$[\![(I,V) \in \mathscr{B}_{IV}]\!]$$

$$\Rightarrow \quad [\![V_{k_1,k_2} + V_{k_2,k_3} + V_{k_3,k_4} + \cdots + V_{k_{n-1},k_n} + V_{k_n,k_1} = 0$$

for all $k_1, k_2, \ldots, k_n \in \{1, 2, \ldots, N\}]\!]$.

KVL

$$\Rightarrow \quad V_{k_1,k_2} = -V_{k_2,k_1} \quad \forall\, k_1, k_2 \in \{1, 2, \ldots, N\}.$$

$$\Leftrightarrow \quad V_{k_1,k_2} + V_{k_2,k_3} + V_{k_3,k_1} = 0$$

$$\forall\, k_1, k_2, k_3 \in \{1, 2, \ldots, N\}.$$

Currents & Potentials

Potentials

Thm: $V : \mathbb{R} \longrightarrow \mathbb{R}^{N \times N}$ **satisfies KVL** $\Leftrightarrow$

$$\exists\, P = \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_N \end{bmatrix} : \mathbb{R} \longrightarrow \mathbb{R}^N \textbf{ such that } V_{k_1,k_2} = P_{k_1} - P_{k_2}.$$

P **'potential'** $\Rightarrow$ $\begin{bmatrix} P_1 + \alpha \\ P_2 + \alpha \\ \vdots \\ P_N + \alpha \end{bmatrix}$ **potential** $\quad \forall\, \alpha : \mathbb{R} \longrightarrow \mathbb{R}.$

Potentials

Thm: $V : \mathbb{R} \longrightarrow \mathbb{R}^{N \times N}$ **satisfies KVL** $\Leftrightarrow$

$$\exists\, P = \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_N \end{bmatrix} : \mathbb{R} \longrightarrow \mathbb{R}^N \textbf{ such that } V_{k_1,k_2} = P_{k_1} - P_{k_2}.$$

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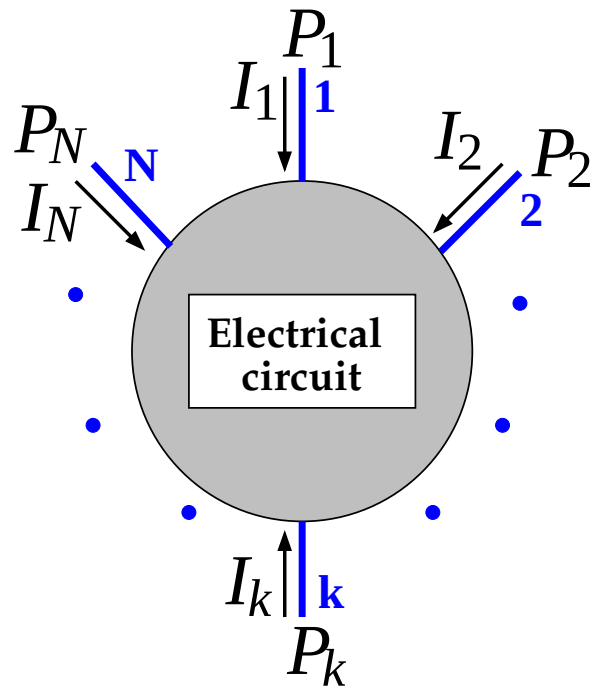
Potentials 'unobservable' from

physically observable currents & voltages.

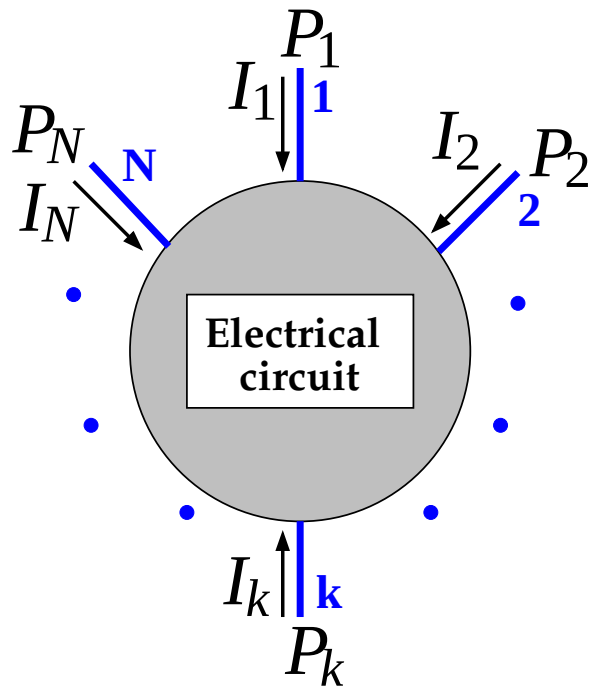
Interaction variables



KVL $\Rightarrow$ at each terminal: a potential and a current

$$\rightsquigarrow \Sigma_{IP} = \left(\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B}_{IP}\right), \quad \mathscr{B}_{IP} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}.$$

Currents and potentials



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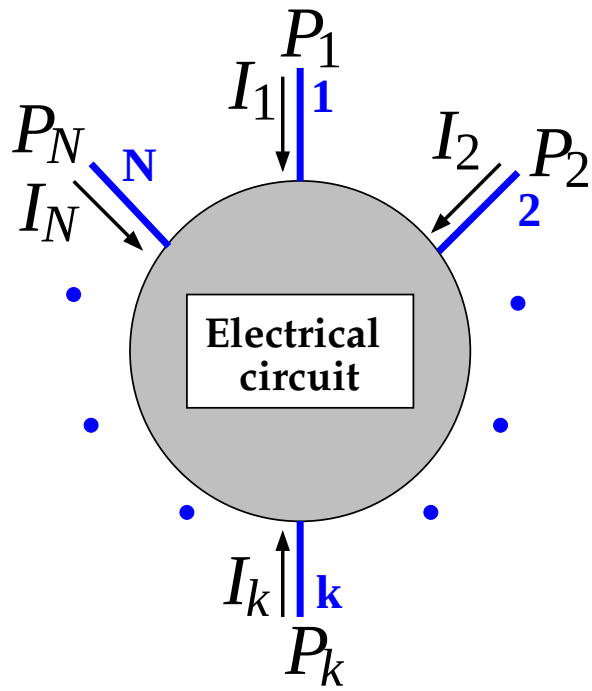
Early sources:

Brockway McMillan

Robert Newcomb

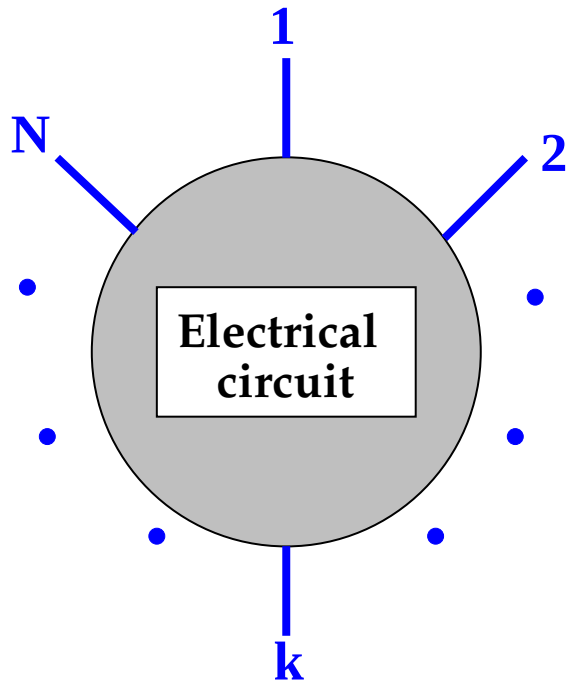
KVL for potentials



Kirchhoff voltage law (KVL):

$$[\![(I_1, I_2, \ldots, I_N, P_1, P_2, \ldots, P_N) \in \mathscr{B}_{IP} \text{ and } \alpha : \mathbb{R} \to \mathbb{R}]\!]$$
$$\Rightarrow [\![\, (I_1, I_2, \ldots, I_N, P_1 + \alpha, P_2 + \alpha, \ldots, P_N + \alpha) \in \mathscr{B}_{IP} \,]\!].$$

KCL



Kirchhoff current law (KCL):

$$[\![(I_1, I_2, \ldots, I_N, V_{1,1}, V_{1,2}, \ldots, V_{k_1,k_2}, \ldots, V_{N,N}) \in \mathscr{B}_{IV}]\!]$$
$$\Rightarrow [\![\, I_1 + I_2 + \cdots + I_N = 0 \,]\!].$$

Assuming KVL, (KCL):

$$[\![(I_1, I_2, \ldots, I_N, P_1, P_2, \ldots, P_N) \in \mathscr{B}_{IP}]\!] \Rightarrow [\![\, I_1 + I_2 + \cdots + I_N = 0 \,]\!].$$

Modeling problem

Given an electrical circuit,

specify the current/voltage behavior

$$\mathscr{B}_{IV} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^{N\times N}\right)^{\mathbb{R}}$$

or, assuming KVL, the current/potential behavior

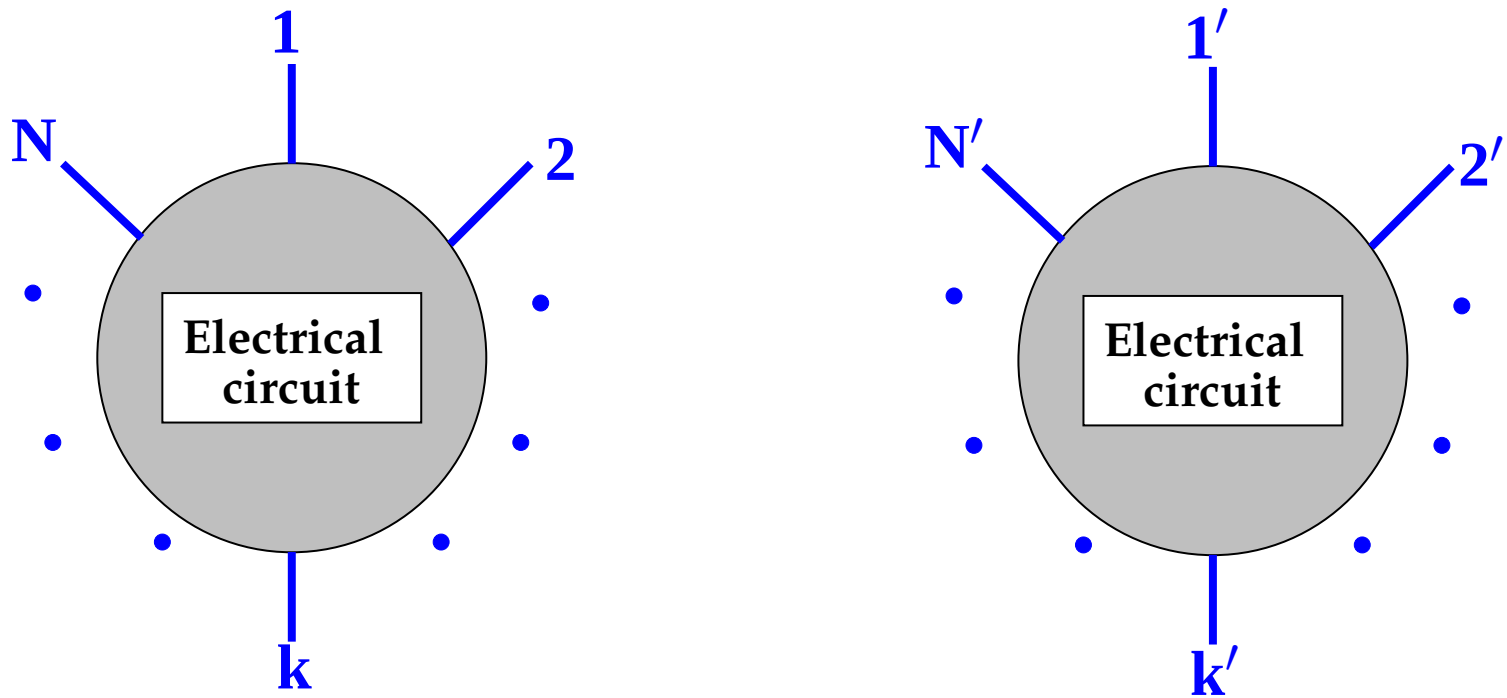
$$\mathscr{B}_{IP} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$$

Related by

$$V_{k_1,k_2} = P_{k_1} - P_{k_2}.$$

New circuits from old ones

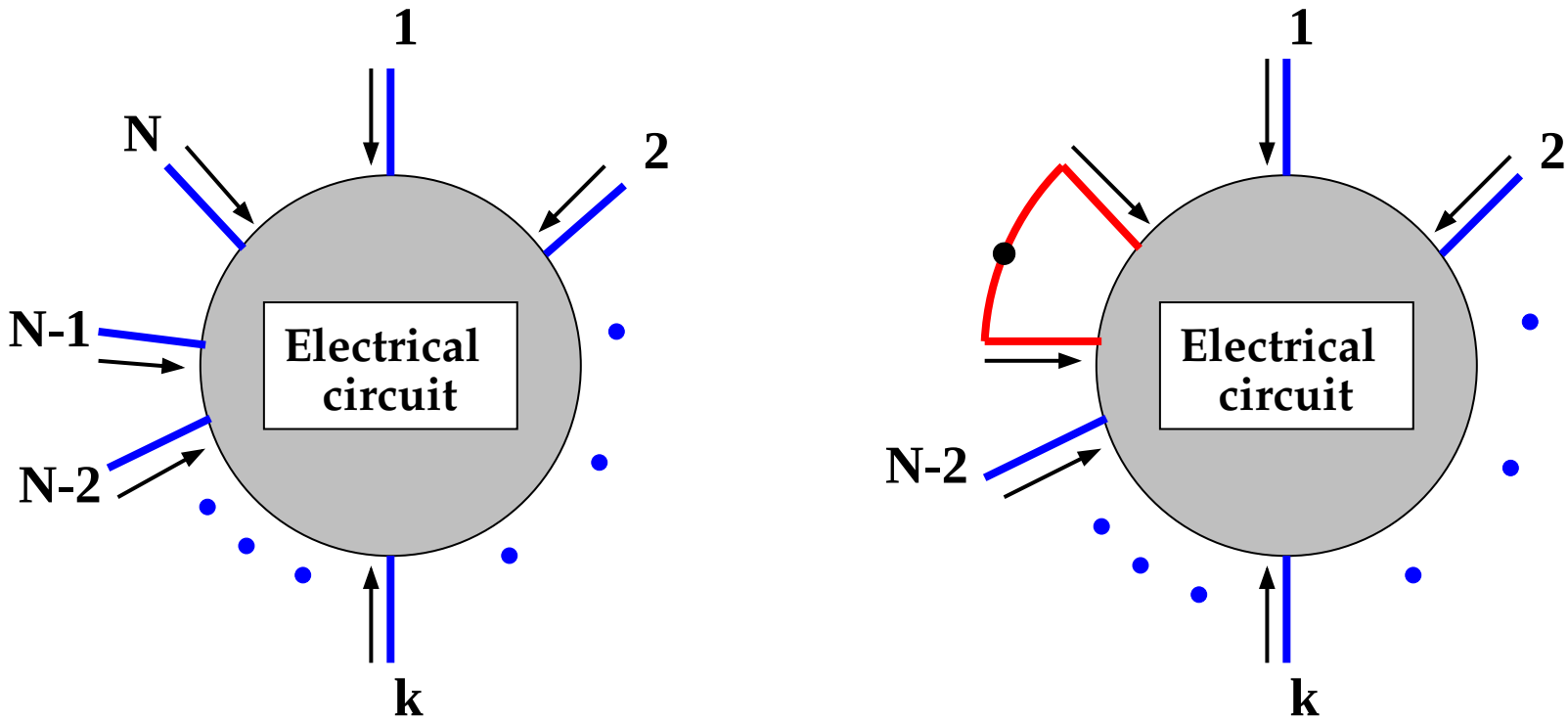
Juxtaposition



$\rightsquigarrow N + N'$ **terminals,** $\mathscr{B}_{IV}^{\text{new}} = \mathscr{B}_{IV} \times \mathscr{B}'_{IV}$.

Preserves KVL and KCL. $\rightsquigarrow$ $\mathscr{B}_{IP}^{\text{new}} = \mathscr{B}_{IP} \times \mathscr{B}'_{IP}$.

Interconnection

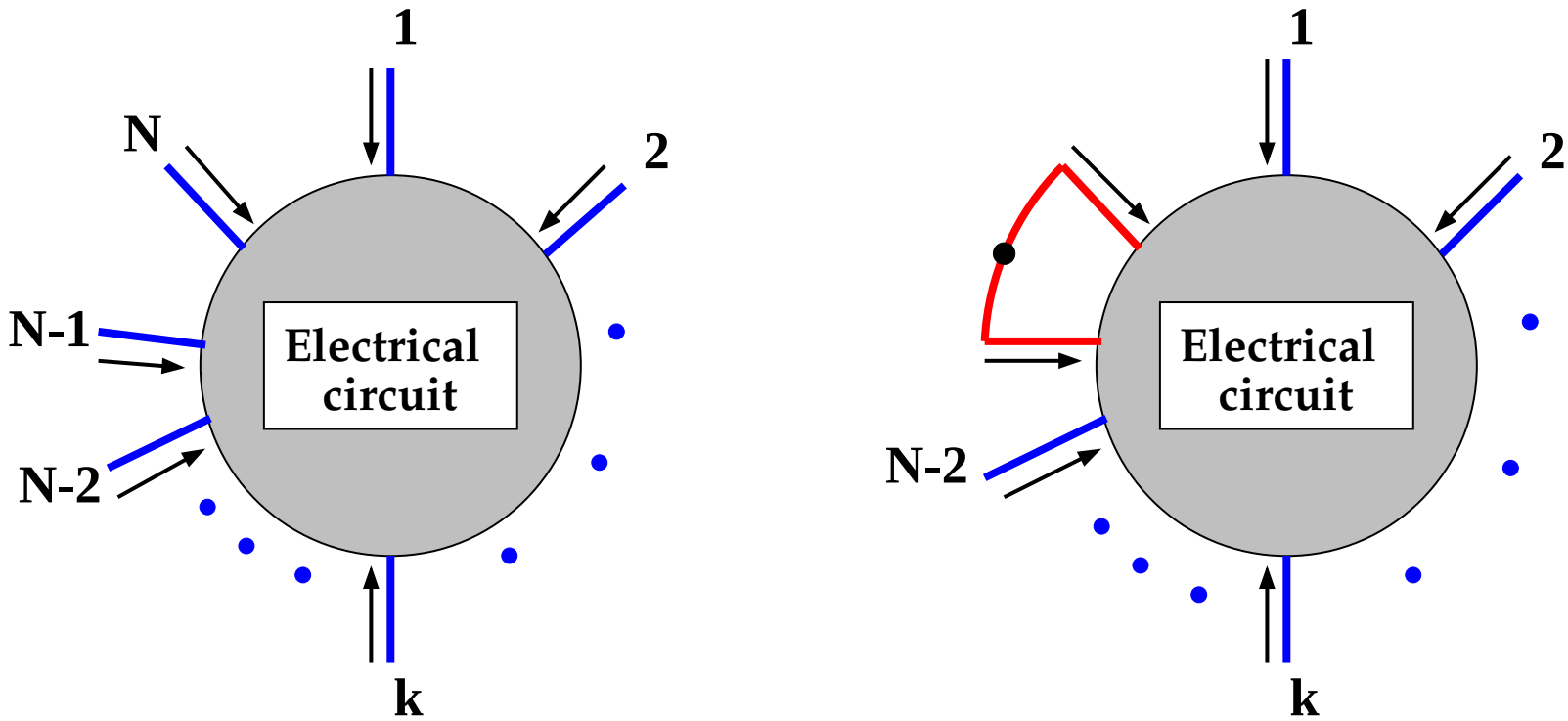


Imposes, in addition to the original behavioral equations,

$V_{N-1,k} = V_{N,k}$ $k = 1, 2, \ldots, N$ **and** $I_{N-1} + I_N = 0.$

$\rightsquigarrow N - 2$ **terminals.** **Preserves KVL and KCL.**

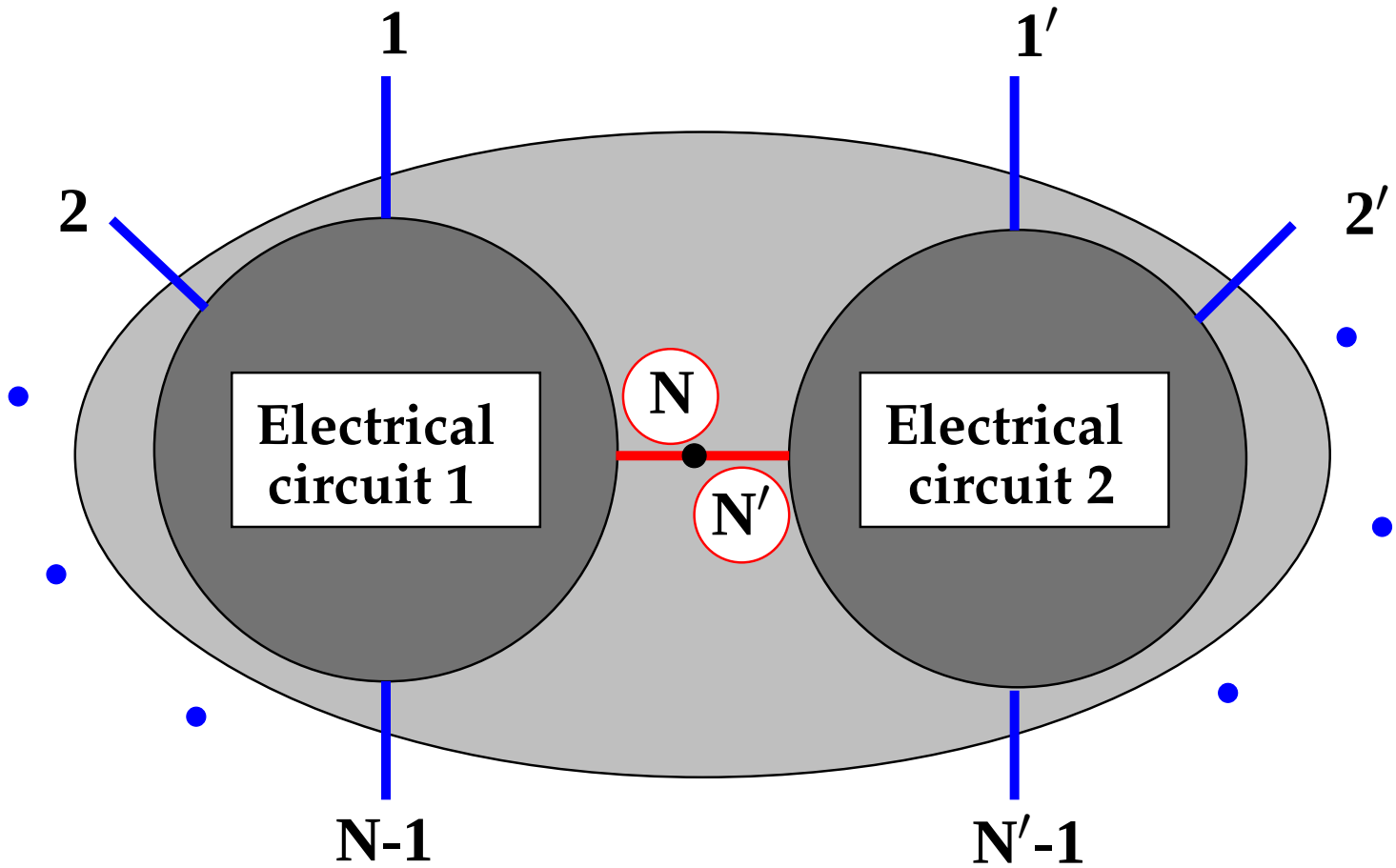
Interconnection



Imposes, in addition to the original behavioral equations, assuming KVL,

$P_{N-1} = P_N$ **and** $I_{N-1} + I_N = 0.$

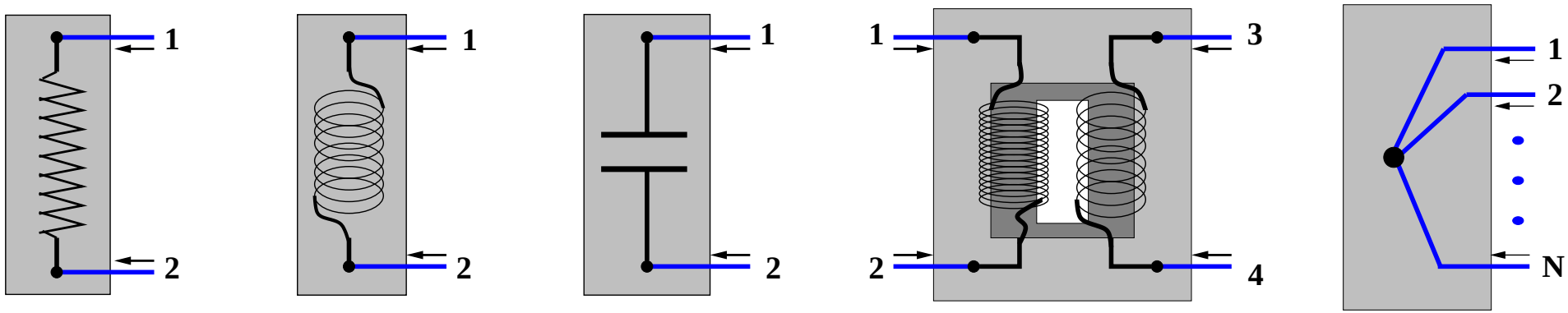
Interconnection



Juxtaposition followed by interconnection. $\rightsquigarrow N + N' - 2$ **terminals.**

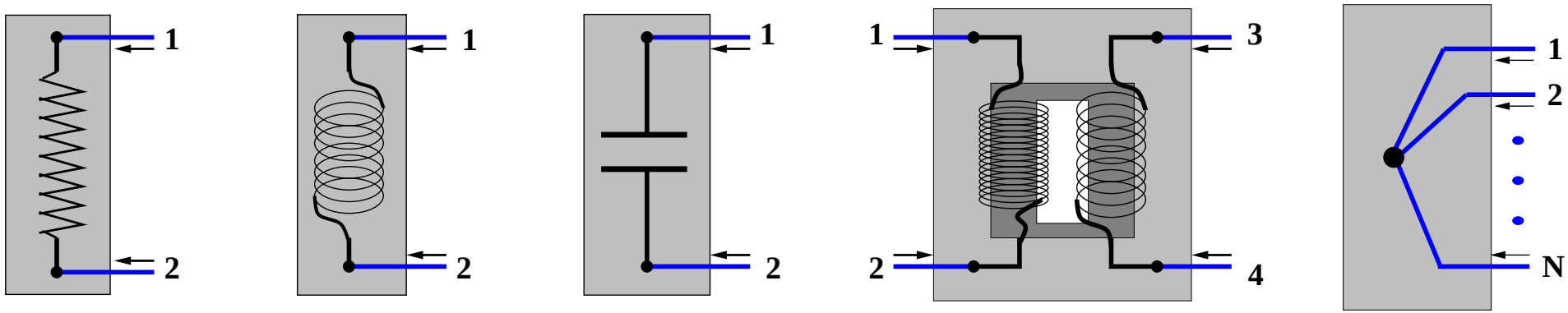
Building blocks

Standard elements



transistors, gyrators, current sources, voltage sources, OPAMPs, ...

Standard elements



transistors, gyrators, current sources, voltage sources, OPAMPs, ...

$$\begin{array}{lrcll} \textbf{resistor:} & P_1 - P_2 & = & R I_1, & I_1 + I_2 = 0, \\ \textbf{inductor:} & P_1 - P_2 & = & L \frac{d}{dt} I_1, & I_1 + I_2 = 0, \\ \textbf{capacitor:} & C \frac{d}{dt}(P_1 - P_2) & = & I_1, & I_1 + I_2 = 0, \end{array}$$

transformer: $P_3 - P_4 = n(P_1 - P_2),\ I_1 = -n I_3, I_1 + I_2 = 0,\ I_3 + I_4 = 0,$

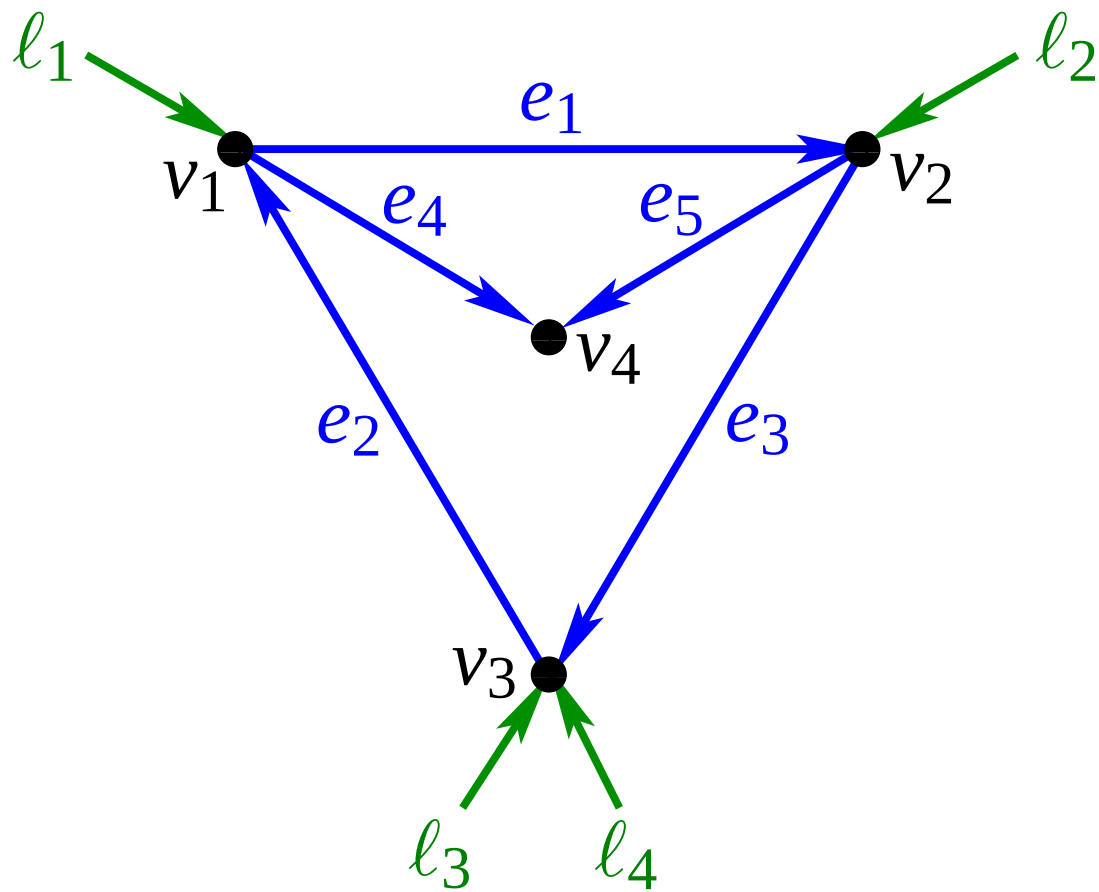
connector: $I_1 + I_2 + \cdots + I_N = 0, \quad P_1 = P_2 = \cdots = P_N.$

How do we formalize the architecture of a circuit, consisting of an interconnection of building blocks?

Digraph with leaves

Digraph with leaves

A digraph with leaves has vertices, edges, and *leaves* (edges incident with ONLY ONE vertex).



Digraph with leaves

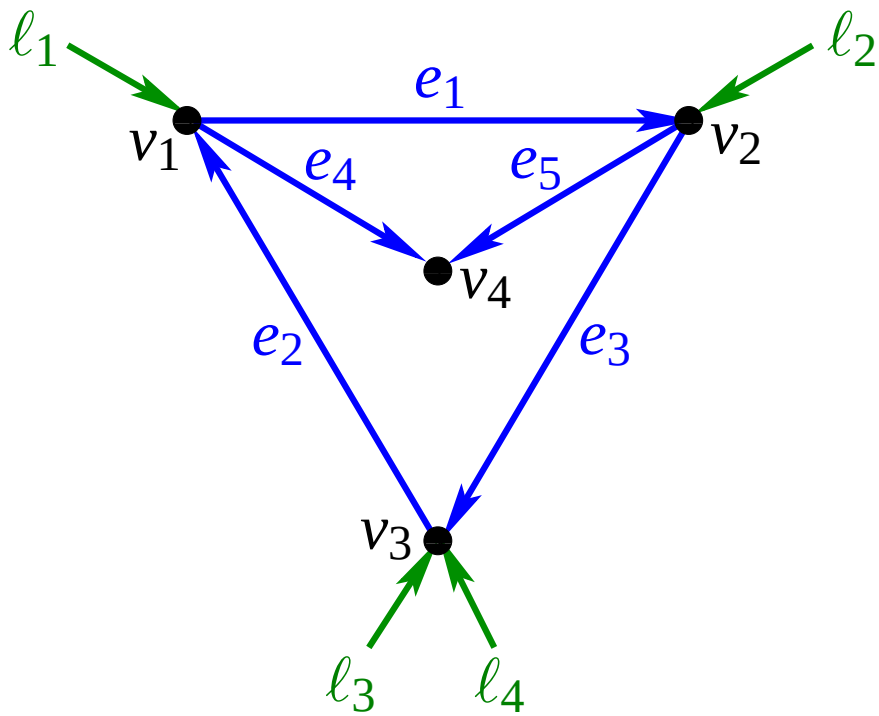
A digraph with leaves has vertices, edges, and *leaves* (edges incident with ONLY ONE vertex).

Mathematically specified by

edge incidence matrix and leaf incidence matrix.

$\{0, +1, -1\}$**-matrices**

Incidence matrices

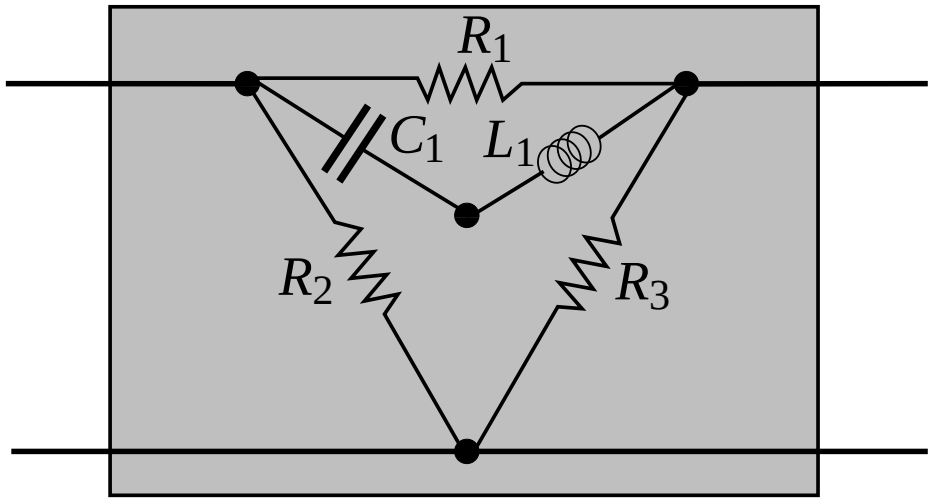


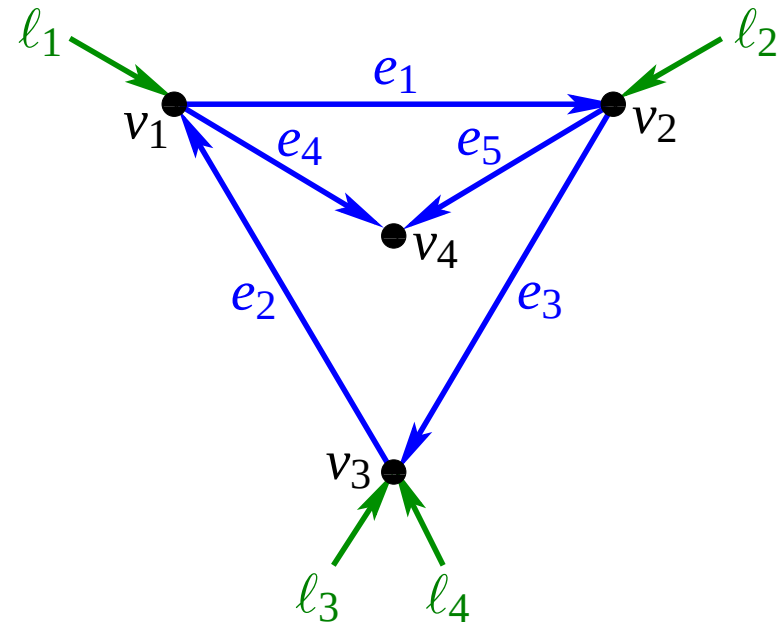
$$\mathbb{V} = \{v_1, v_2, v_3, v_4\}$$
$$\mathbb{E} = \{e_1, e_2, e_3, e_4, e_5\}$$
$$\mathbb{L} = \{\ell_1, \ell_2, \ell_3, \ell_4\}$$

$$\mathbb{A}_{\mathbb{E}} = \begin{bmatrix} +1 & -1 & 0 & +1 & 0 \\ -1 & 0 & +1 & 0 & +1 \\ 0 & +1 & -1 & 0 & 0 \\ 0 & 0 & 0 & -1 & -1 \end{bmatrix}, \quad \mathbb{A}_{\mathbb{L}} = \begin{bmatrix} -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

RLC circuits

Circuit architecture





Circuit architecture :=

digraph with leaves $\cong$ $(\mathbb{A}_{\mathbb{E}}, \mathbb{A}_{\mathbb{L}})$

Element specification

The elements of the circuit (the R's, L's, and C's) correspond to the edges.

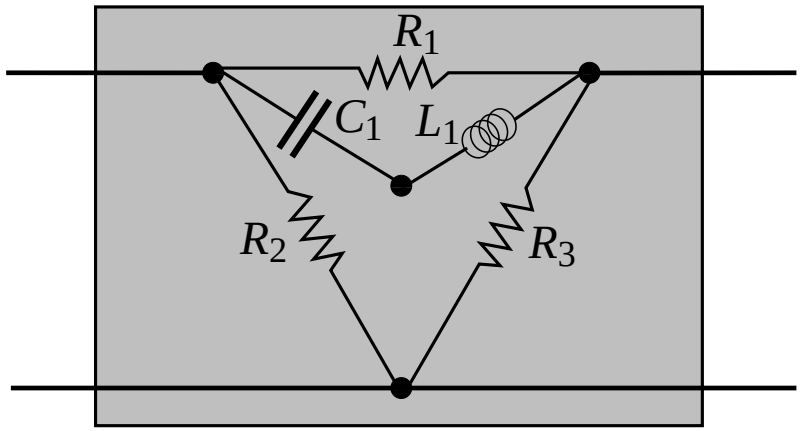
$\rightsquigarrow$ **a map that associates with each edge a resistance, an inductance, or a capacitance of a given value.**

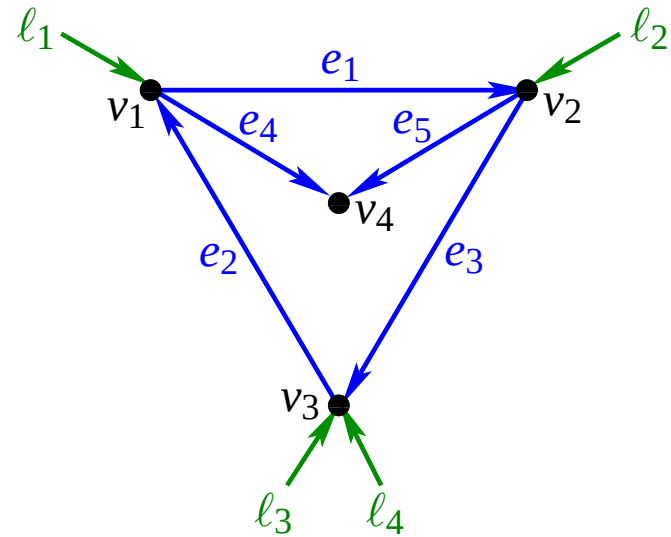
$\rightsquigarrow$

3 $|\mathbb{E}| \times |\mathbb{E}|$ **diagonal matrices** R, L, C

$\Rightarrow$ $|\mathbb{E}| \times |\mathbb{E}|$ **diagonal polynomial matrices** $RL(\xi)$ **and** $C(\xi)$**.**

Element specification





$$RL(\xi) = \begin{bmatrix} R_1 & 0 & 0 & 0 & 0 \\ 0 & R_2 & 0 & 0 & 0 \\ 0 & 0 & R_3 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & L_1\xi \end{bmatrix}, \quad C(\xi) = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & C_1\xi & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}.$$

Circuit equations

Manifest variables:

the leaf currents I and the leaf potentials P.

Latent variables:

the edge currents $I_{\mathbb{E}}$ and the vertex potentials $P_{\mathbb{V}}$.

$$I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{|\mathbb{L}|} \end{bmatrix}, \quad P = \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_{|\mathbb{L}|} \end{bmatrix}, \quad I_{\mathbb{E}} = \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ \vdots \\ I_{e_{|\mathbb{E}|}} \end{bmatrix}, \quad P_{\mathbb{V}} = \begin{bmatrix} P_{v_1} \\ P_{v_2} \\ \vdots \\ P_{v_{|\mathbb{V}|}} \end{bmatrix}.$$

Circuit equations

Edges $\rightsquigarrow$ **constitutive equations for each edge:**

$$RL\left(\frac{d}{dt}\right) I_{\mathbb{E}} = C\left(\frac{d}{dt}\right) A_{\mathbb{E}}^{\top} P_{\mathbb{V}}.$$

Vertices $\rightsquigarrow$ **KCL for each vertex:**

$$A_{\mathbb{E}} I_{\mathbb{E}} + A_{\mathbb{L}} I = 0.$$

Leaves $\rightsquigarrow$ **potential assignment for each leaf:**

$$P + A_{\mathbb{L}}^{\top} P_{\mathbb{V}} = 0.$$

Circuit properties

- **Elimination of $I_{\mathbb{E}}$ and $P_{\mathbb{V}}$ $\Rightarrow$ for $\mathscr{B}_{IP}$**

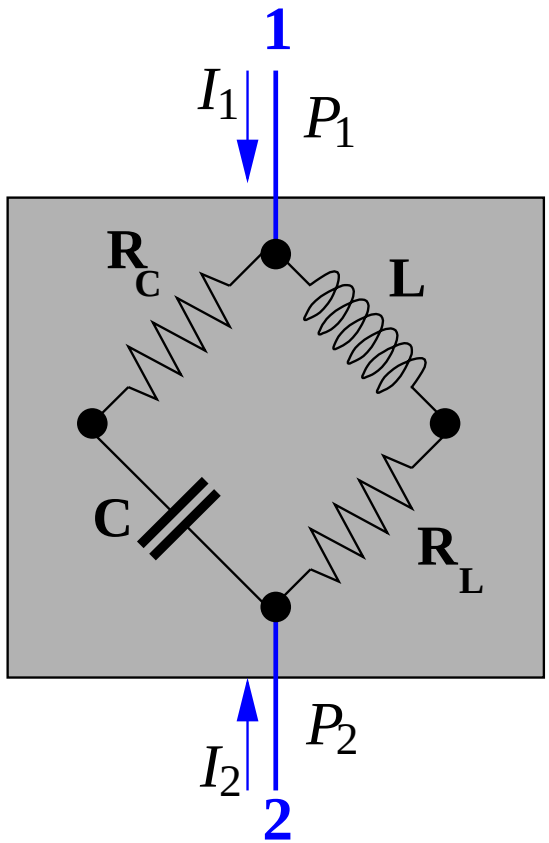
$$F\left(\frac{d}{dt}\right)\begin{bmatrix} I \\ P \end{bmatrix} = 0, \qquad F \in \mathbb{R}[\xi]^{\bullet \times 2N}.$$

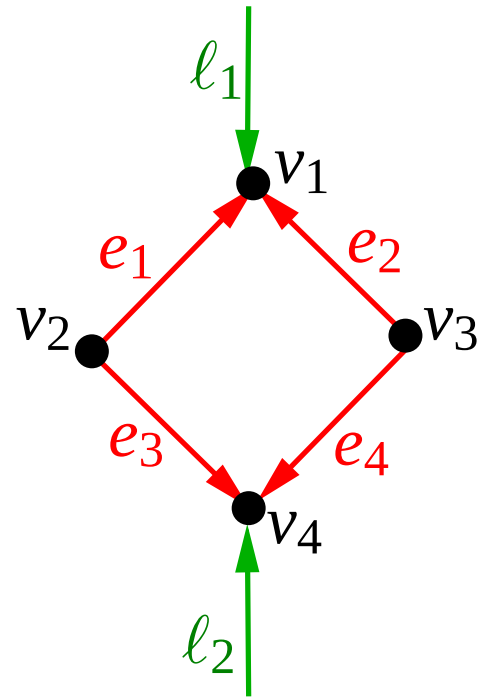
- **KVL and KCL**
- **Passivity**
- **Hybridicity**
- **Reciprocity**
- **etc.**

Modeling methodology

- **Generalizes to 2-terminal 1-ports in edges**
- **Generalizes to 2-terminal multi-ports in edges**
- **Generalizes to nonlinear circuits**
- **Restricted to 2-terminal ports**

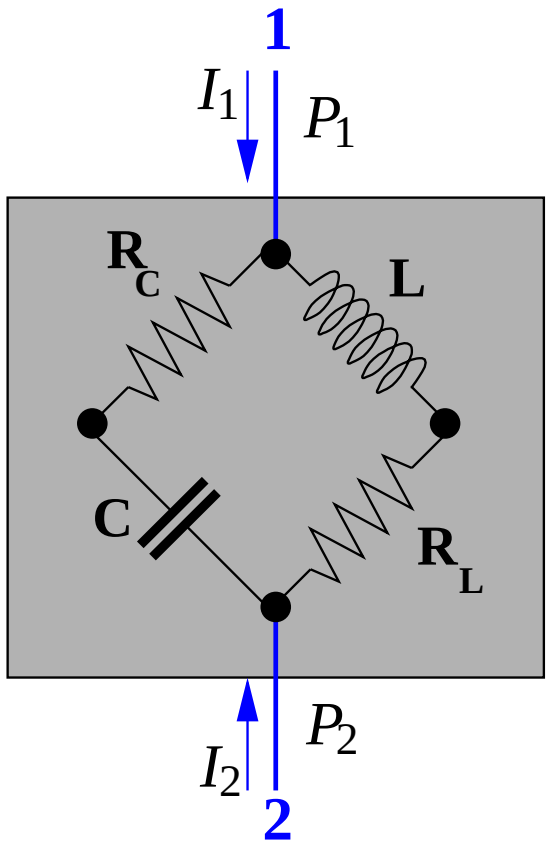
Example

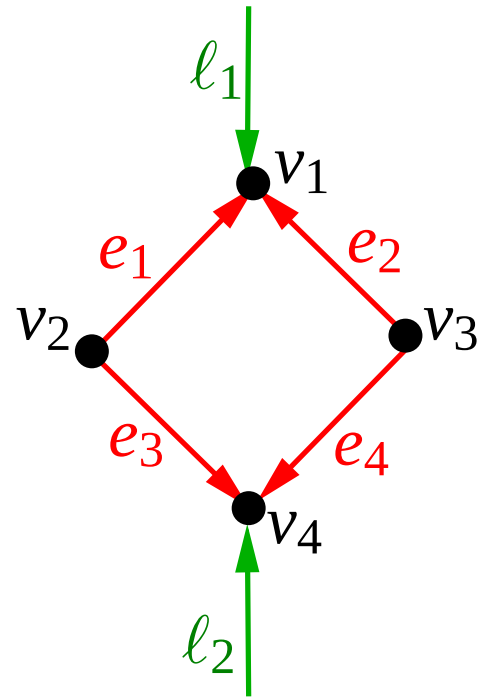




$$\mathbb{A}_{\mathbb{V}} = \begin{bmatrix} -1 & -1 & 0 & 0 \\ +1 & 0 & +1 & 0 \\ 0 & +1 & 0 & +1 \\ 0 & 0 & -1 & -1 \end{bmatrix}, \qquad \mathbb{A}_{\mathbb{L}} = \begin{bmatrix} -1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1 \end{bmatrix}.$$

Example





$$I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, P = \begin{bmatrix} P_1 \\ P_2 \end{bmatrix}, \qquad I_{\mathbb{E}} = \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ I_{e_3} \\ I_{e_4} \end{bmatrix}, P_{\mathbb{V}} = \begin{bmatrix} P_{v_1} \\ P_{v_2} \\ P_{v_3} \\ P_{v_4} \end{bmatrix}.$$

Behavioral equations

$$\begin{bmatrix} R_C & 0 & 0 & 0 \\ 0 & L\frac{d}{dt} & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & R_L \end{bmatrix} \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ I_{e_3} \\ I_{e_4} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & C\frac{d}{dt} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} -P_{v_1} + P_{v_2} \\ -P_{v_1} + P_{v_3} \\ P_{v_2} - P_{v_4} \\ P_{v_3} - P_{v_4} \end{bmatrix},$$

$$\begin{bmatrix} I_{e_1} + I_{e_2} + I_1 = 0 \\ I_{e_1} + I_{e_3} = 0 \\ I_{e_2} + I_{e_4} = 0 \\ I_{e_3} + I_{e_4} + I_2 = 0 \end{bmatrix}, \qquad \begin{bmatrix} P_1 = P_{v_1} \\ P_2 = P_{v_4} \end{bmatrix}.$$

Elimination of $I_{\mathbb{E}}$ and $P_{\mathbb{V}} \rightsquigarrow$ (trust me!):

The circuit behavior

$\rightsquigarrow$ **the following ODE defines $\mathscr{B}_{IP}$.**

Case 1: $CR_C \neq \dfrac{L}{R_L}$.

$$\left(\frac{R_C}{R_L}+\left(1+\frac{R_C}{R_L}\right)CR_C\frac{d}{dt}+CR_C\frac{L}{R_L}\frac{d^2}{dt^2}\right)(P_1-P_2)$$
$$=\left(1+CR_C\frac{d}{dt}\right)\left(1+\frac{L}{R_L}\frac{d}{dt}\right)R_C I_1,$$

$$I_1+I_2=0.$$

The circuit behavior

$\rightsquigarrow$ **the following ODE defines $\mathscr{B}_{IP}$.**

Case 2: $CR_C = \dfrac{L}{R_L}$.

$$\left(\frac{R_C}{R_L} + CR_C\frac{d}{dt}\right)(P_1 - P_2) = \left(1 + CR_C\frac{d}{dt}\right)R_C I_1,$$

$$I_1 + I_2 = 0.$$

The circuit behavior

$\rightsquigarrow$ **the following ODE defines $\mathscr{B}_{IP}$.**

Case 2: $CR_C = \dfrac{L}{R_L}$.

$$\left(\frac{R_C}{R_L} + CR_C\frac{d}{dt}\right)(P_1 - P_2) = \left(1 + CR_C\frac{d}{dt}\right)R_C I_1,$$

$$I_1 + I_2 = 0.$$

$$CR_C = \frac{L}{R_L} \text{ and } R_C = R_L \quad \Leftrightarrow \quad \text{uncontrollable.}$$

Hence: Linear passive circuits can become uncontrollable.

Common factors

$CR_C \neq \dfrac{L}{R_L}$ **and** $CR_C \to \dfrac{L}{R_L} \rightsquigarrow$ **a common factor.**

It should be cancelled in $CR_C = \dfrac{L}{R_L}$**!**

$CR_C = \dfrac{L}{R_L}$ **and** $R_C = R_L \rightsquigarrow$ **a second common factor.**

This one should not be cancelled.

That is what the math gives (trust me!).

Common factors

Suppose we work with the impedance, and cancel common factors. Is this OK?

$CR_C = \dfrac{L}{R_L}$ **and** $R_C = R_L \rightsquigarrow$

$$\left(\frac{R_C}{R_L} + CR_C\frac{d}{dt}\right)V) = \left(1 + CR_C\frac{d}{dt}\right)R_C I.$$

After cancellation $\rightsquigarrow \qquad V = R_C I.$

Short circuit ($V = 0$**)** $\rightsquigarrow$

$$\left(1 + CR_C\frac{d}{dt}\right)R_C I = 0 \ \textbf{versus} \ I = 0.$$

Observable exponentials disappear. Here exponentially stable, but could be only stable, then surely bothersome.

Consequences

For an exact, complete description of the physics of an RLC circuit, the impedance does not suffices.

Requires a bit of rethinking of Thévenin, Norton, Seshu, even classical synthesis, ...

Synthesis problem

Informal formulation

Given a system, a *behavior*, and a set of *building blocks*,
find an *architecture* and an *embedding* of building blocks
such that the interconnected system realizes the given behavior.

We take a look at the following classical case:

- **behavior : a linear time-invariant differential (LTID) current/voltage behavior,**
- **building blocks : linear *passive* resistors, inductors, capacitors, and transformers**
  $\rightsquigarrow$ RLCT synthesis.

Pedigree

Ronald Foster

Wilhelm Cauer

Otto Brune

Raoul Bott & Richard Duffin

Bernard Tellegen

Brockway McMillan

Vitold Belevitch

Sidney Darlington

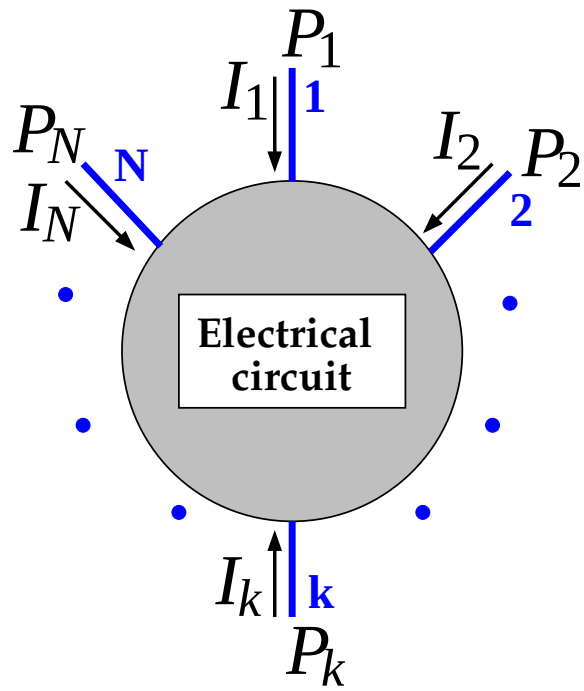
Dante Youla

and many others...

We add some footnotes to the work of these EE pioneers...

N-terminal circuits

Currents and potentials



At each terminal: a current and a potential

$$\rightsquigarrow \textbf{behavior } \mathscr{B}_{IP} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$$

Elimination thm. $\rightsquigarrow$ **RLCT circuit $\Rightarrow$ LTID behavior**

Synthesis

For which polynomial matrices $F \in \mathbb{R}[\xi]^{\bullet \times 2N}$ is

$$F\left(\frac{d}{dt}\right)\begin{bmatrix} I \\ P \end{bmatrix} = 0$$

the terminal behavior $\mathscr{B}_{IP}$ of an RLCT circuit?

¡¡ ***Given such an $F \in \mathbb{R}[\xi]^{\bullet \times 2N}$,***
specify an RLCT circuit that has this terminal behavior $\mathscr{B}_{IP}$ **!!**

Further cases of interest:

allow only: RLC, R, RC, RL, LC, RT, etc.

Our two footnotes

- **Do we want to realize the *correct behavior***
  or only the *correct controllable part* ?

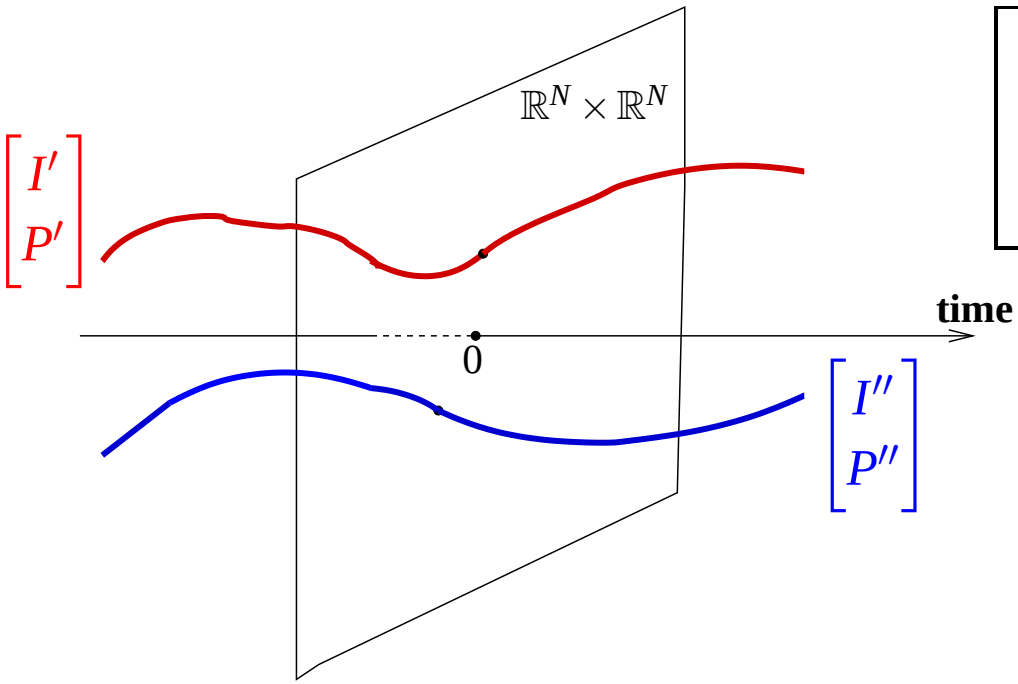
Our two footnotes

- **Do we want to realize the *correct behavior***
  or only the *correct controllable part*?

- **Do we want to realize an N-*terminal* circuit,**
  or an N-*port* circuit?

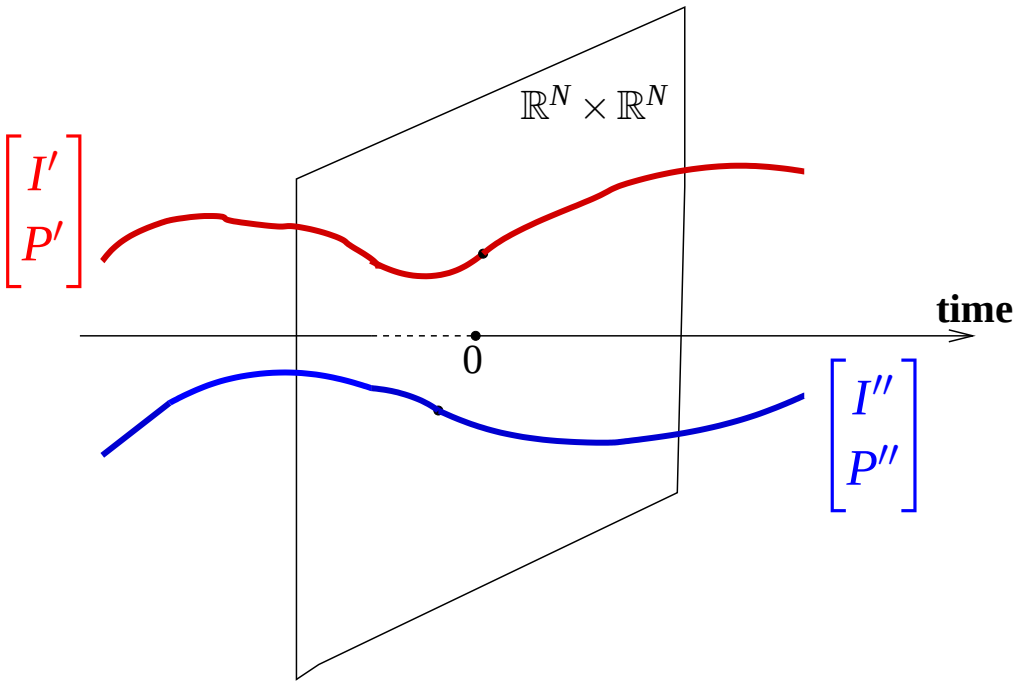
Controllability

Definition of controllability

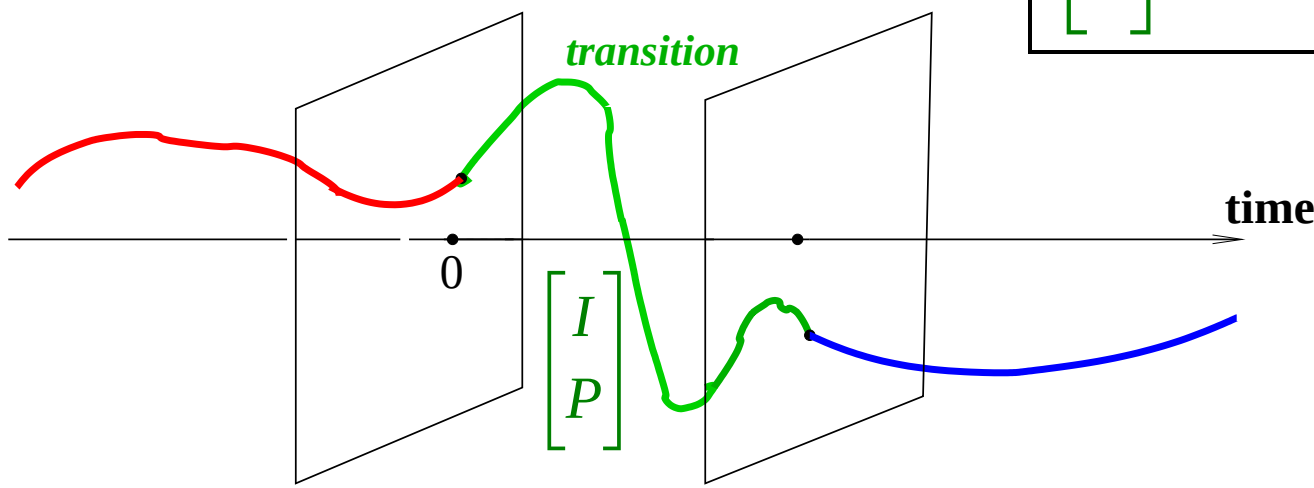


$$\begin{bmatrix} I' \\ P' \end{bmatrix}, \begin{bmatrix} I'' \\ P'' \end{bmatrix} \in \mathscr{B}_{IP}$$

Definition of controllability



$$\begin{bmatrix} I \\ P \end{bmatrix} \in \mathscr{B}_{IP}$$



controllability :$\Leftrightarrow$ concatenability of trajectories after a delay .

Controllability of LTIDSs

The following are equivalent for $F\left(\frac{d}{dt}\right)\begin{bmatrix} I \\ P \end{bmatrix} = 0$**.**

- $\mathscr{B}_{IP}$ **is controllable.**
- F **(WLOG full row rank) is left prime.**
- **...**

Controllability of LTIDSs

The following are equivalent for $F\left(\frac{d}{dt}\right)\begin{bmatrix} I \\ P \end{bmatrix} = 0$**.**

- $\mathscr{B}_{IP}$ **is controllable.**
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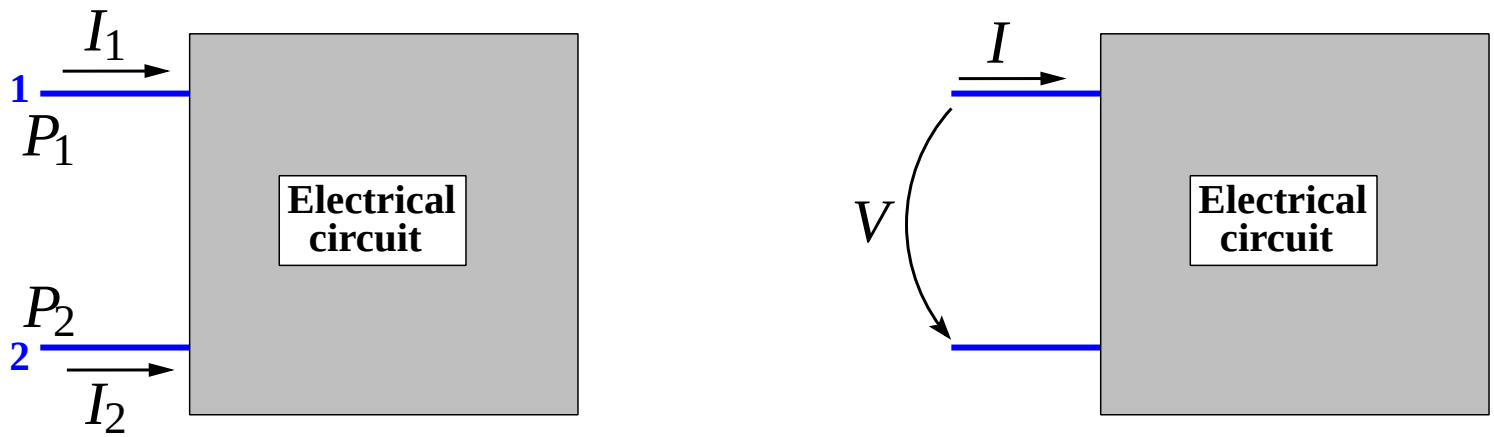
- **...**

The RLC example which we worked out shows

uncontrollable circuits are not degenerate.

Realization of 2-terminal circuits

2-terminal circuits



KCL $\Rightarrow I_1 + I_2 = 0,$ **KVL** $\Rightarrow$ **only** $P_1 - P_2$ **matters.**

with $I := I_1 = -I_2$ **and** $V := P_1 - P_2$**, this leads to**

$$P\left(\frac{d}{dt}\right) V = Q\left(\frac{d}{dt}\right) I\,.$$

Define $Z := \dfrac{Q}{P}$ ***'impedance'***.

2-terminal circuits

$$P\left(\frac{d}{dt}\right)V = Q\left(\frac{d}{dt}\right)I, \qquad Z = \frac{Q}{P}.$$

Which polynomial pairs (P, Q) are realizable
using RLCT? Using RLC?

2-terminal circuits

$$P\left(\frac{d}{dt}\right)V = Q\left(\frac{d}{dt}\right)I\,, \qquad Z = \frac{Q}{P}\,.$$

Which polynomial pairs (P,Q) are realizable
using RLCT? Using RLC?

Assume P and Q are coprime ($\Leftrightarrow$ controllability).
Then RLCT realizable iff Z is positive real (Brune).

Iff Z is positive real,
then the controllable part is RLCT realizable (Brune).

Iff Z is positive real, then there exists RLC realization
with the 'correct' controllable part (Bott-Duffin).
Bott-Duffin introduces uncontrollably common factors.
Are they Hurwitz? I do not know. Perhaps not!

Open problem

Which polynomial pairs (P, Q) are realizable using RLCT?

Necessary condition 1: $Z = \dfrac{Q}{P}$ **is positive real.**

Necessary condition 2: Uncontrollable part 'stable'.

1 + 2 are not sufficient.

Sufficient condition: P **and** Q **coprime, and** $Z = \dfrac{Q}{P}$ **p.r.**

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Sufficient condition: P **and** Q **coprime, and** $Z = \dfrac{Q}{P}$ **p.r.**

Conclusions:

The set of RLCT realizable LTID behaviors is unknown.

Bott-Duffin realizes the impedance, but not the behavior.

Example 1

$$\frac{d}{dt}V = \frac{d^2}{dt^2}I$$

has impedance ξ: positive real. Common factor ξ: stable.

Not realizable.

Proof: the short-circuit behavior is

$$\frac{d^2}{dt^2}I = 0,$$

which is not stable! And that violates passivity.

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Example 2

There is presently no theory that guarantees that

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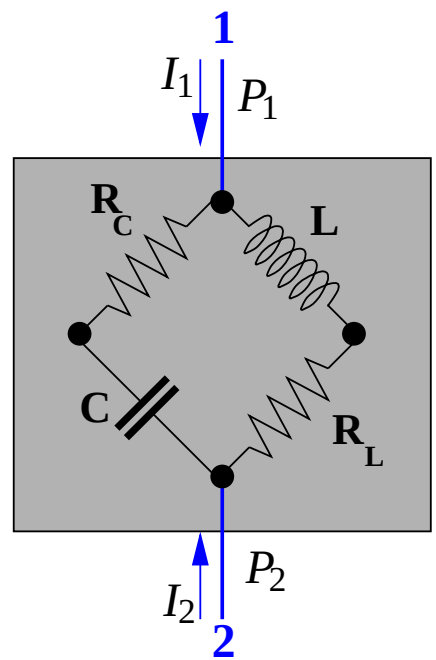
is realizable.

Example 2

There is presently no theory that guarantees that

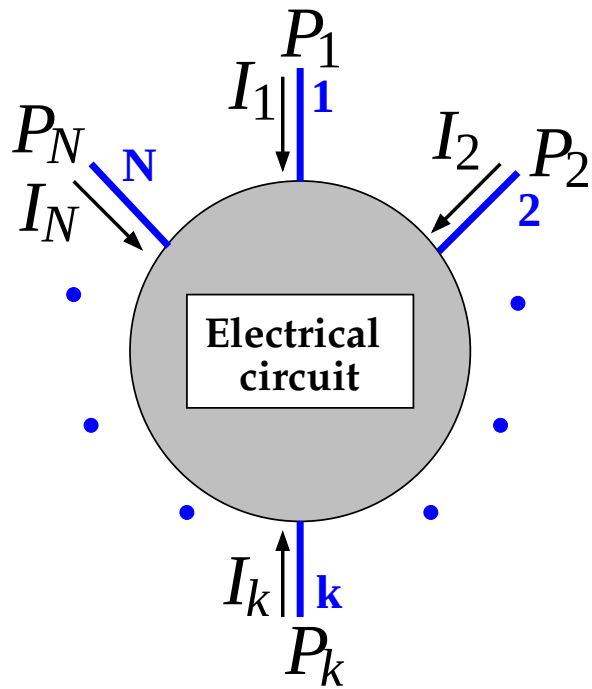
$$\left(1+\frac{d}{dt}\right)V = \left(1+\frac{d}{dt}\right)I,$$

is realizable. But it is, using $R_C = R_L = 1, C = 1, L = 1$**.**



N-port versus N-terminal circuits

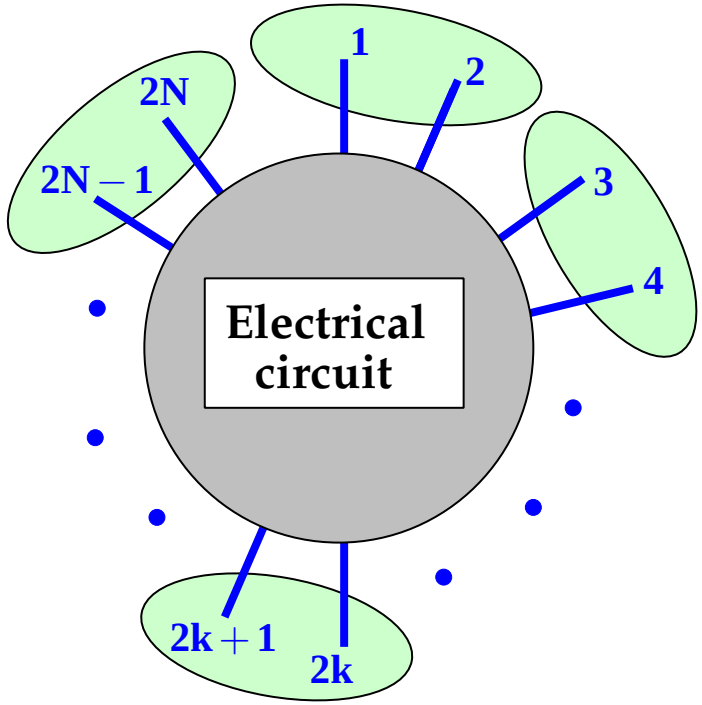
N-terminal circuit



At each terminal: a current and a potential

$$\rightsquigarrow \boldsymbol{\Sigma} = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B}_{IP}) \quad \textbf{behavior } \mathscr{B}_{IP} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$$

N-port



$2N$-terminal circuit.
Assume KVL.
behavior $\mathscr{B}_{IP} \subseteq \left(\mathbb{R}^{2N} \times \mathbb{R}^{2N}\right)^{\mathbb{R}}$

Pair the terminals, set

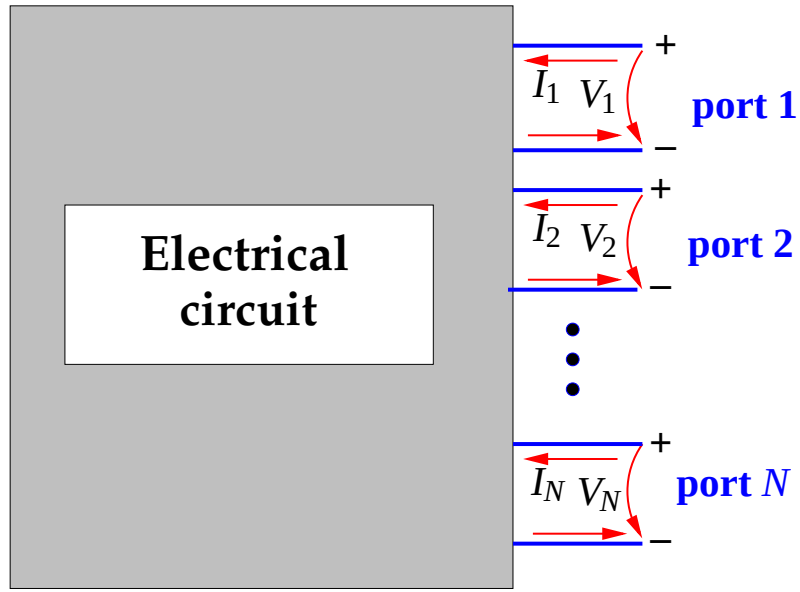
$$I_1 + I_2 = 0, \;\; I_3 + I_4 = 0, \cdots, I_{2N-1} + I_{2N} = 0,$$

and take as variables the *'port' currents* and *'port' voltages*

$$I'_1 = I_1, \;\; I'_2 = I_3, \cdots, I'_N = I_{2N-1},$$

$$V_1 = P_1 - P_2, \;\; V_2 = P_3 - P_4, \cdots, V_N = P_{2N-1} - P_{2N}.$$

Currents and voltages



$\rightsquigarrow \Sigma_{\text{port}} = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B}_{\text{port}})$ **port behavior** $\mathscr{B}_{\text{port}} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$

$(I_1, I_2, \ldots, I_N, V_1, V_2, \ldots, V_N) : \mathbb{R} \to \mathbb{R}^N \times \mathbb{R}^N \in \mathscr{B}_{\text{port}}$ **means:**

this current/voltage trajectory is compatible with $\mathscr{B}_{IP}$ *and the port current constraints*.

Classical synthesis problem

Given a LTID behavior $\mathscr{B}_{\text{port}} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$**,**

find a $2N$**-terminal RLCT circuit with** N**-port behavior** $\mathscr{B}_{\text{port}}$**.**

Classical synthesis problem

Given a LTID behavior $\mathscr{B}_{\text{port}} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$,
find a $2N$-terminal RLCT circuit with N-port behavior $\mathscr{B}_{\text{port}}$.

- **For the 2-terminal case, KCL and KVL imply that 1-port synthesis is equivalent to 2-terminal synthesis.**
- ***If transformers are allowed* in the synthesis, then the results of the N-port case and the N-terminal case are transferrable.**
  Modulo controllability, a RLCT synthesis exists iff, roughly, the multivariable impedance is symmetric and positive real.
- **Without transformers, the N-port and the N-terminal cases are distinct.**

Resistive terminal synthesis

Transformerless resistive synthesis

The synthesis of resistive N-ports without transformers is one of the open problems of classical N-port synthesis.

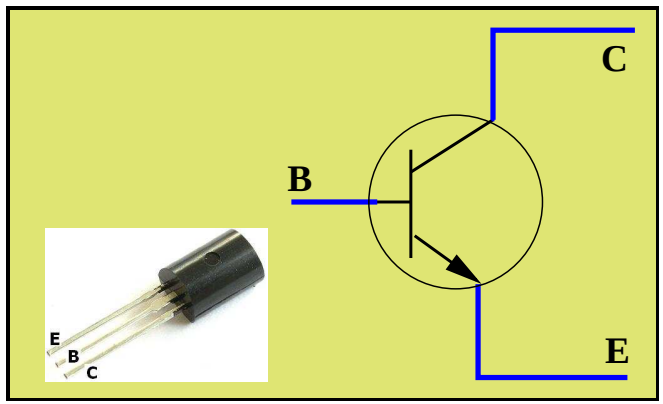
For N-terminal synthesis, it can be solved completely.

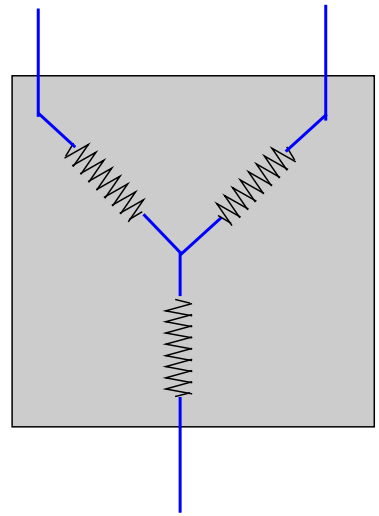
Interconnected circuits

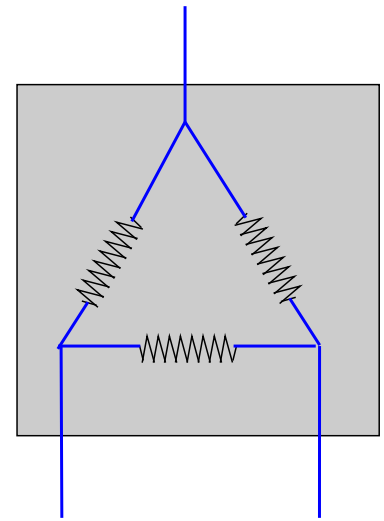
3-terminal circuits

Classical graph and digraph methods are restricted to elements with 2-terminal ports.

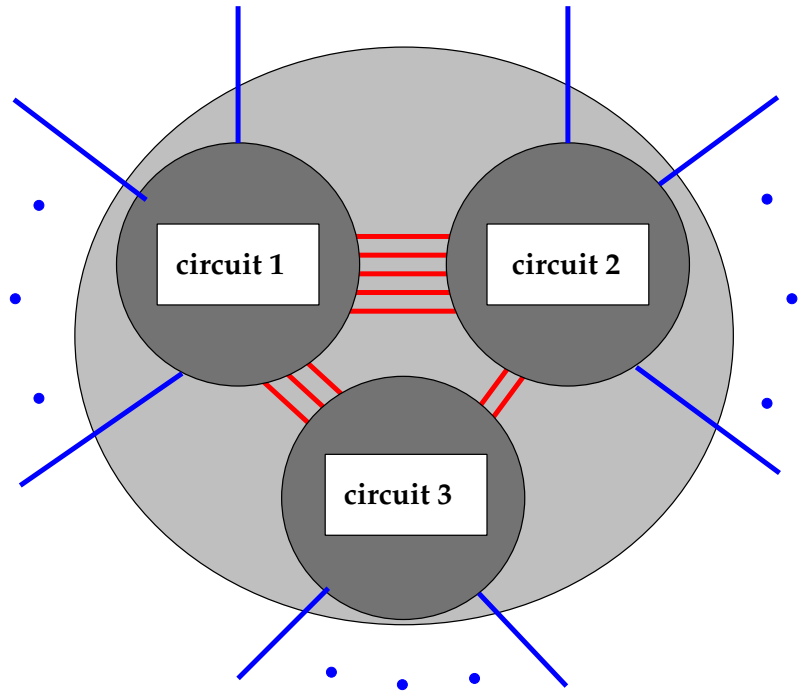
They do not deal with 3-terminal circuits, such as





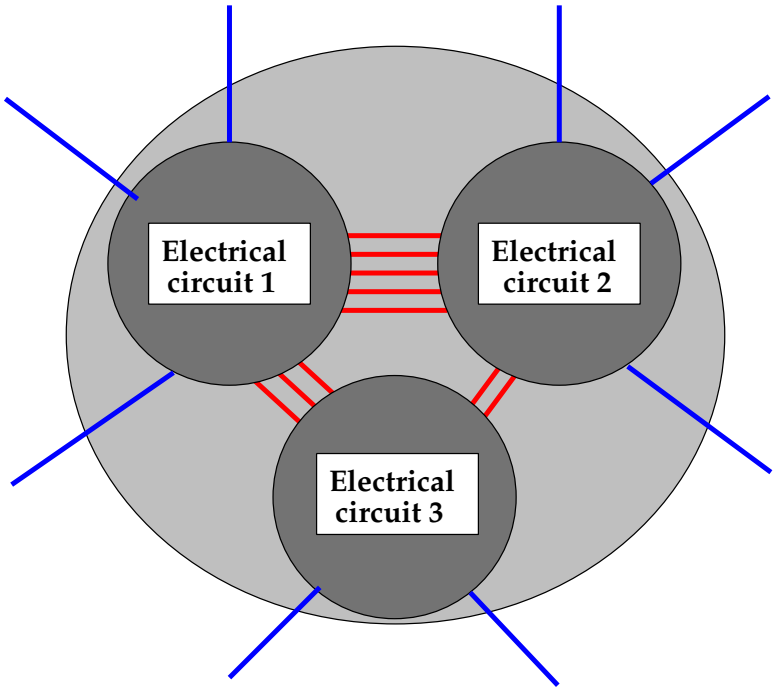


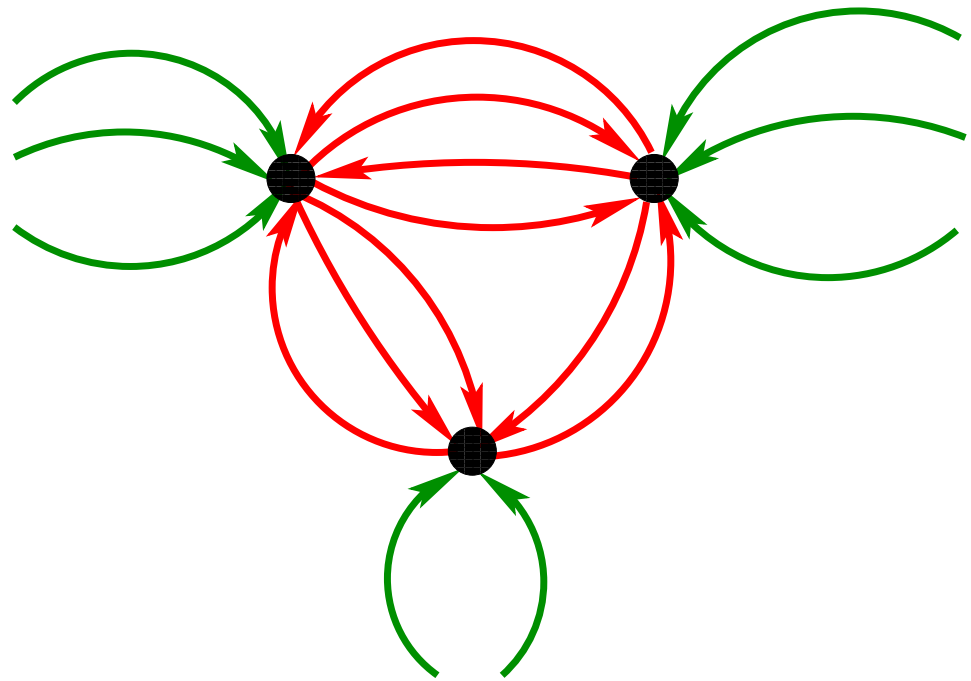
Interconnected multiterminal circuits



We outline a hierarchical method that incorporates multi-terminal ports and general interconnected circuits.

Interconnection architecture





Tearing, zooming, & linking

Interconnection architecture: graph with leaves

- Subcircuits in the vertices
- Connections in the edges
- External terminals in the leaves

Tearing, zooming, & linking

Interconnection architecture: graph with leaves

- **Subcircuits in the vertices**
- **Connections in the edges**
- **External terminals in the leaves**

Contrast with classical view

- **Connections in vertices**
- **Subcircuits in edges**

Interconnection architecture

Manifest variables:

the leaf currents I and the leaf potentials P.

Latent variables:

the edge currents $I_{\mathbb{E}}$ and the edge potentials $P_{\mathbb{E}}$.

$$I = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{|\mathbb{L}|} \end{bmatrix}, \quad P = \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_{|\mathbb{L}|} \end{bmatrix}, \quad I_{\mathbb{E}} = \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ \vdots \\ I_{e_{|\mathbb{E}|}} \end{bmatrix}, \quad P_{\mathbb{E}} = \begin{bmatrix} P_{e_1} \\ P_{e_2} \\ \vdots \\ P_{e_{|\mathbb{E}|}} \end{bmatrix}.$$

External behavior

- **Behavior for each vertex**

  involves $I, P,\ I_{\mathbb{E}}, P_{\mathbb{E}}$**.**

- **Interconnection equation for each edge**

  involves $I_{\mathbb{E}}, P_{\mathbb{E}}$**.**

$$I_{e_{\text{side1}}} + I_{e_{\text{side2}}} = 0, \quad P_{e_{\text{side1}}} = P_{e_{\text{side2}}}$$

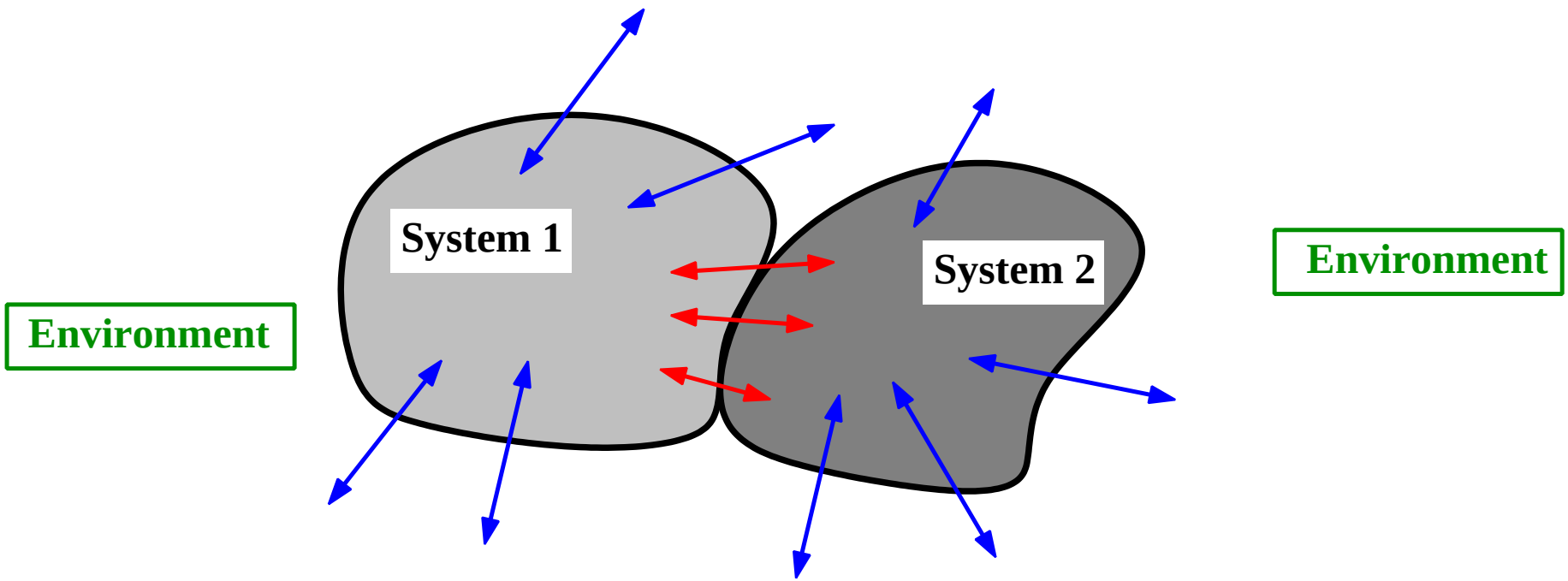
- $\rightsquigarrow$ **behavioral equations in** $I, P,\ I_{\mathbb{E}}, P_{\mathbb{E}}$**.**

- **Eliminate edge currents** $I_{\mathbb{E}}$ **and edge potentials** $P_{\mathbb{E}}$

  $\rightsquigarrow$ **behavioral equations for** I, P**.**

Energy Transfer

Theme



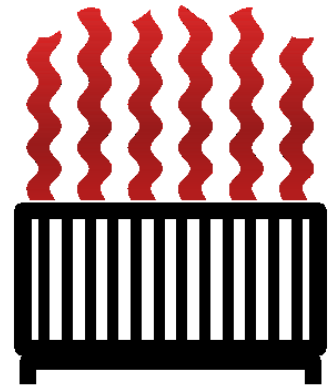
How is energy transferred from the environment to a system?

How is energy transferred between systems?

Does interconnection mean energy transfer?

Energy

Energy := a physical quantity transformable into heat.



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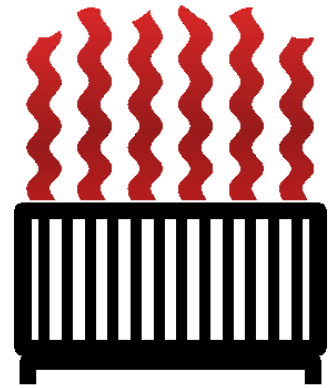
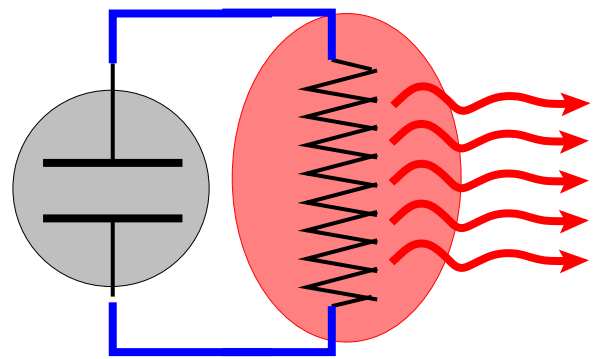


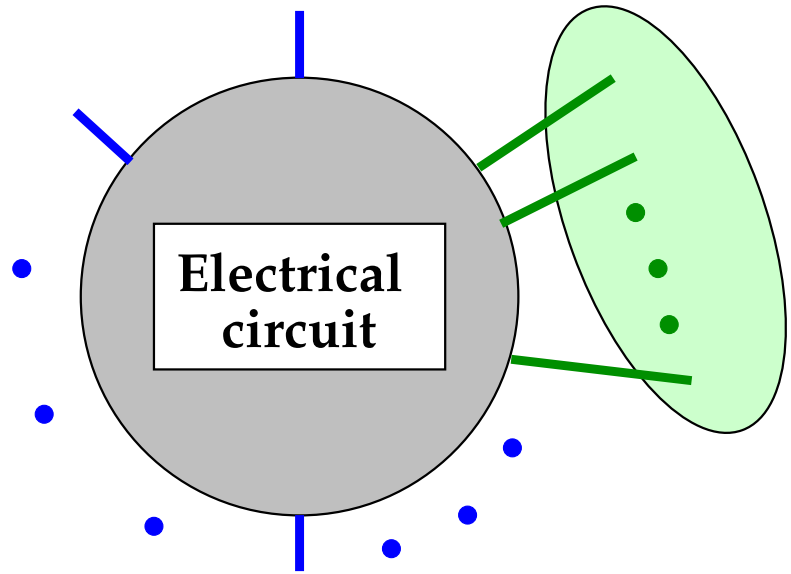
For example, capacitor $\mapsto$ resistor $\mapsto$ heat.

Energy on capacitor = $\frac{1}{2}CV^2$



Electrical ports

Energy transfer

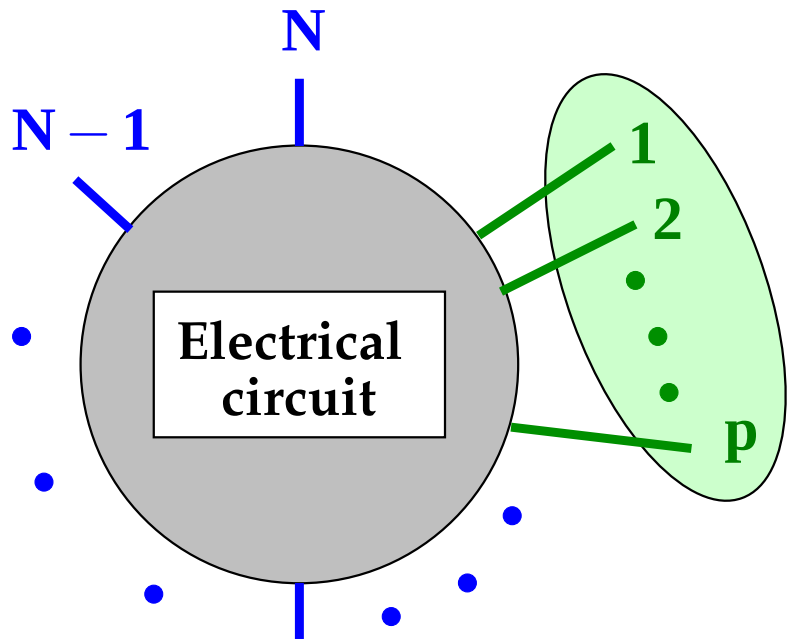


Environment

Assume that we monitor the current/potential on a set of terminals.

Can we speak about *'the energy transferred from the environment to the circuit along these terminals'*?

Ports



Assume henceforth KVL.

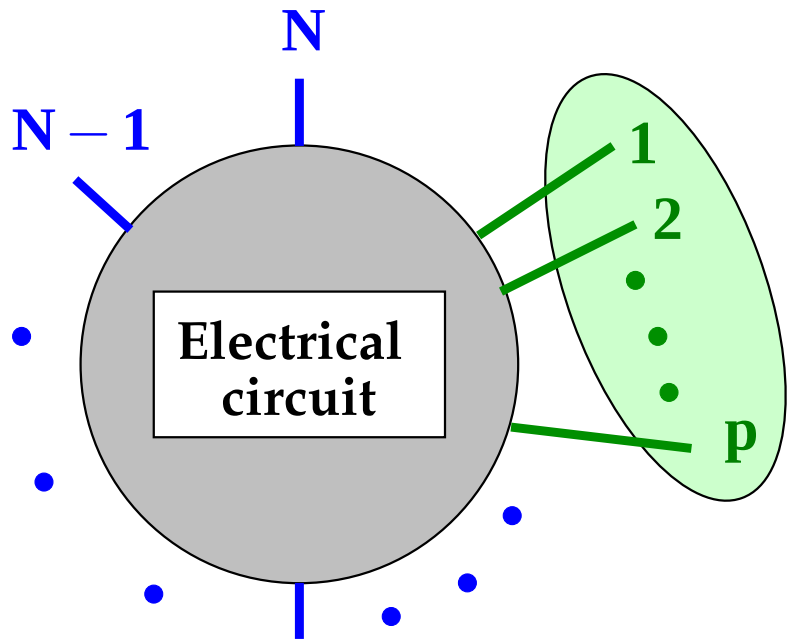
Terminals $\{1,2,\ldots,p\}$ **form a port** $:\Leftrightarrow$

$$[\![(I_1,\ldots,I_p,I_{p+1},\ldots,I_N,P_1,\ldots,P_p,P_{p+1},\ldots,P_N,) \in \mathscr{B}_{IP}]\!]$$

$$\Rightarrow \quad [\![\, I_1+I_2+\cdots+I_p=0 \,]\!]. \qquad \textit{'port KCL'}$$

KCL $\Rightarrow$ all terminals together form a port.

Ports



If terminals $\{1, 2, \ldots, p\}$ form a port, then

power **in =** $P_1(t)I_1(t) + P_2(t)I_2(t) + \cdots + P_p(t)I_p(t)$

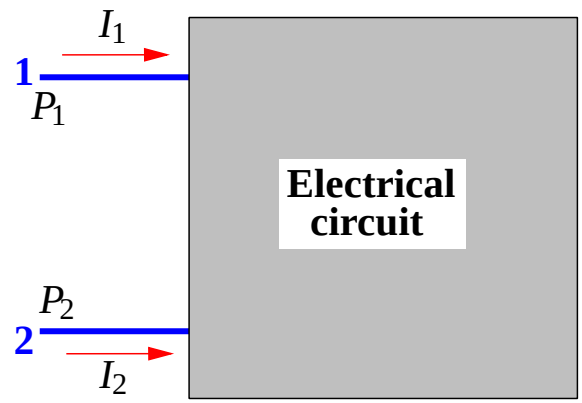
energy **in =** $\displaystyle\int_{t_1}^{t_2} [P_1(t)I_1(t) + P_2(t)I_2(t) + \cdots + P_p(t)I_p(t)]\, dt$

This interpretation in terms of power and energy is not valid unless these terminals form a port !

Examples

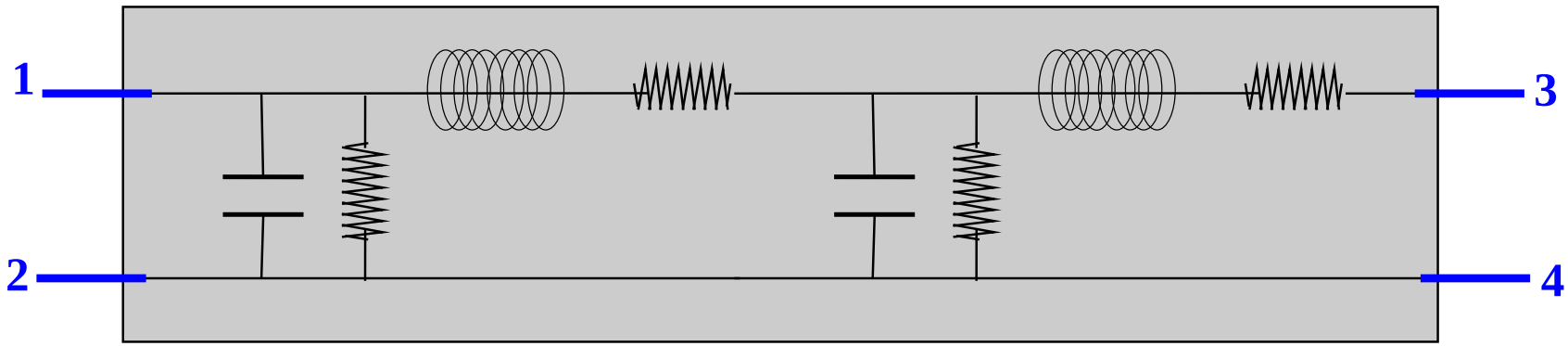
2-terminal 1-port devices:

resistors, inductors, capacitors, memristors, etc.,
any 2-terminal circuit composed of these.



KCL $\Rightarrow$ **a port** $(I_1 = -I_2 =: I)$.
KVL $\Rightarrow$ **only** $P_1 - P_2 =: V$ **matters.**
$\rightsquigarrow$ **usual circuit variables** (I, V)**.**

Example

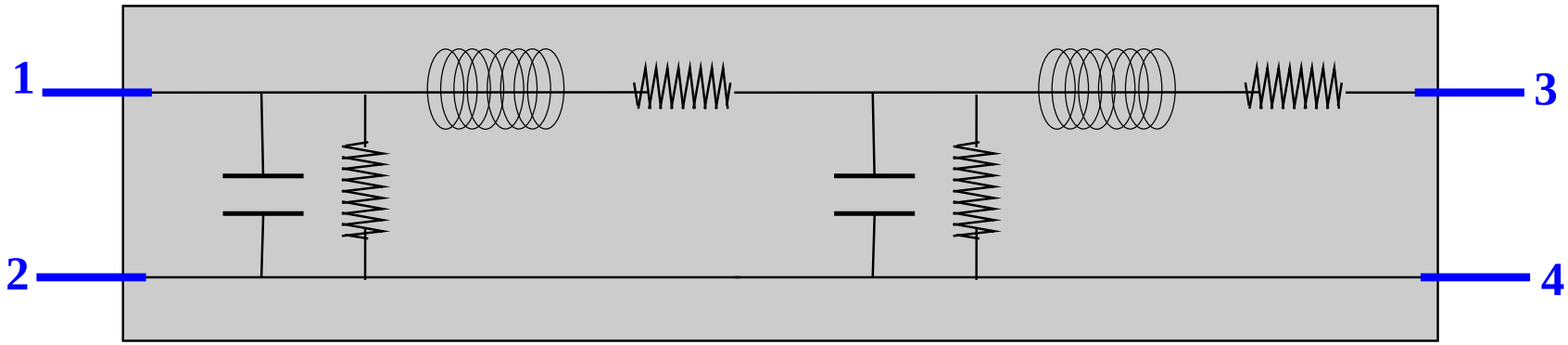


Terminals $\{1,2,3,4\}$ form a port. But $\{1,2\}$ and $\{3,4\}$ do not.

We cannot speak about

***'the energy transferred from terminals $\{1,2\}$ to $\{3,4\}$'*.**

Example



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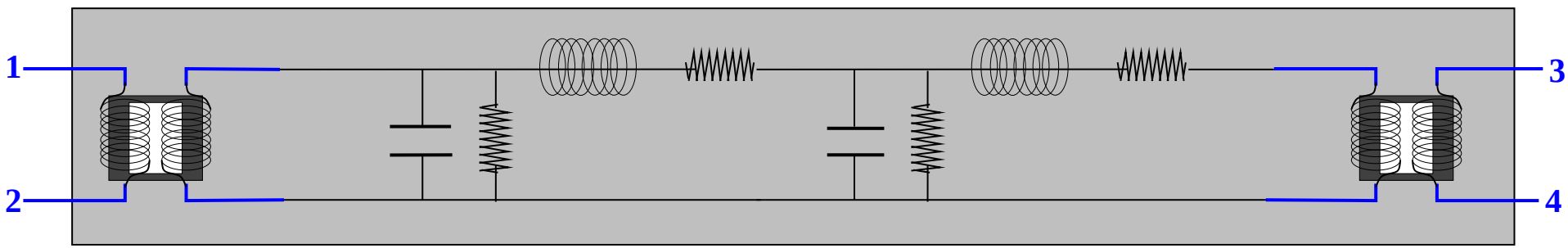
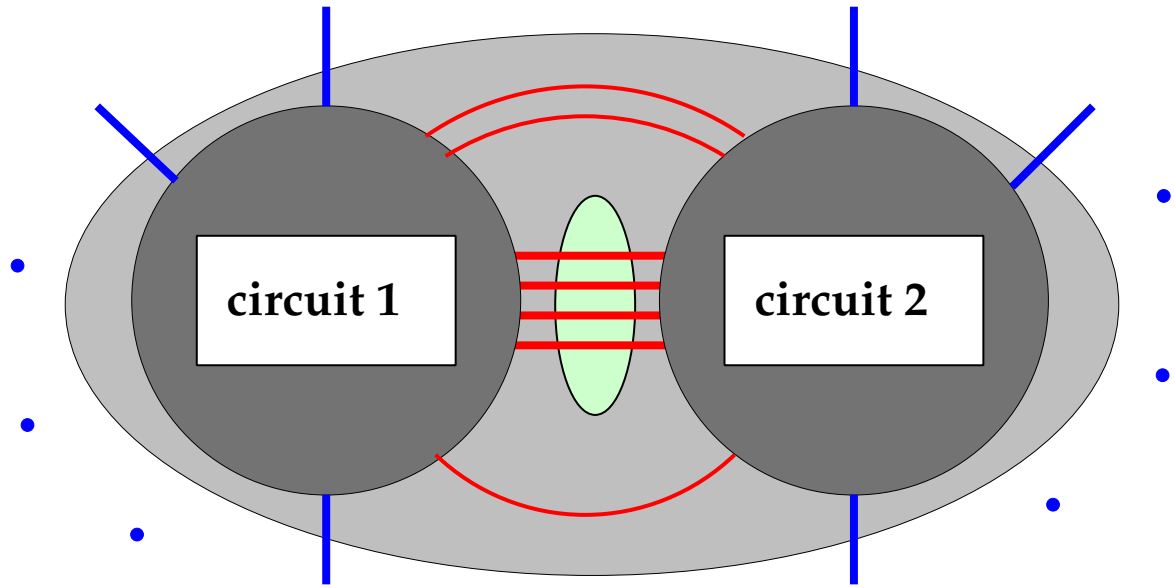


Terminals $\{1,2\}$ and $\{3,4\}$ form ports.

Energy transfer between circuits

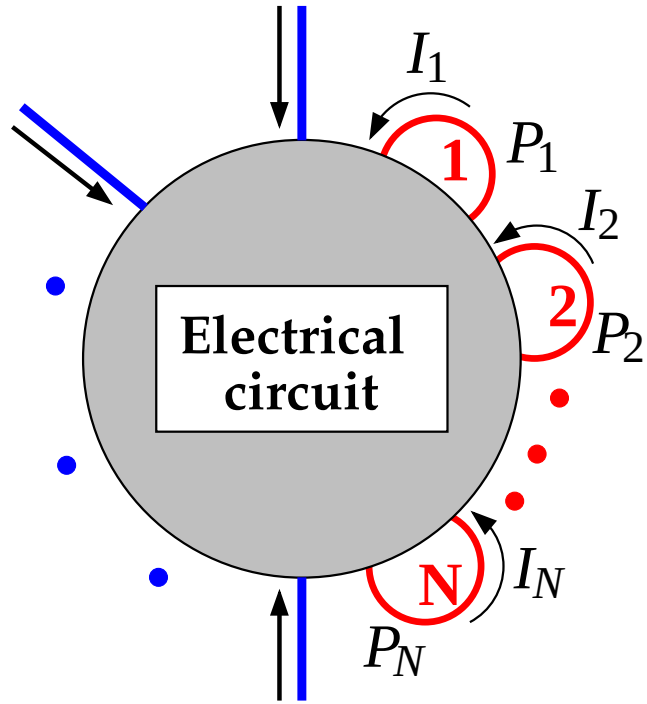


Assume that we monitor the current/potential on a set of terminals between circuits or within a circuit.

Can we speak about

***'the energy transferred along these terminals'*?**

Internal ports



Terminals $\{1,2,\ldots,N\}$ **form an** **internal port** $:\Leftrightarrow$

$$[\![\,(I_1,I_2,\ldots,I_N,P_1,P_2,\ldots,P_N)\in\mathscr{B}_{IP}\,]\!]$$
$$\Rightarrow [\![\, I_1+I_2+\cdots+I_N=0\,]\!].$$

'internal port-KCL'

Power and energy

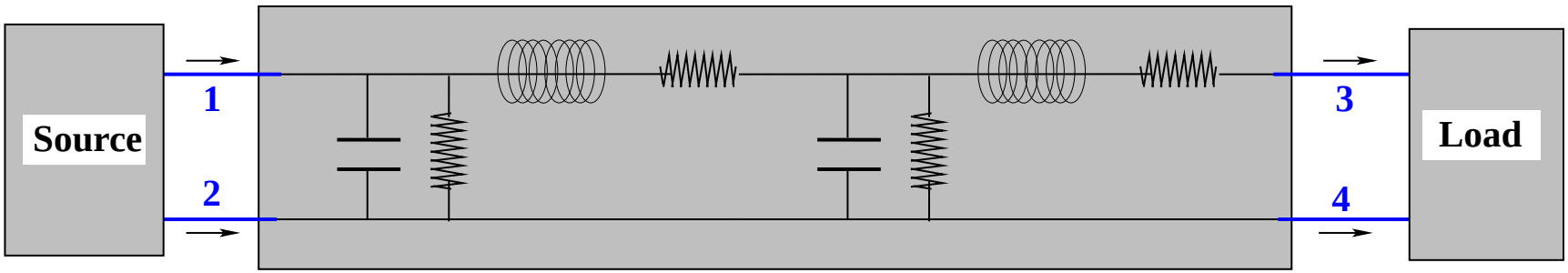
Flow through the terminals *from one side to the other* in the direction of the arrows:

power = $I_1(t)P_1(t) + I_2(t)P_2(t) + \cdots + I_N(t)P_N(t)$

energy = $\displaystyle\int_{t_1}^{t_2} [I_1(t)P_1(t) + I_2(t)P_2(t) + \cdots + I_N(t)P_N(t)]\, dt$

This physical interpretation of power and energy is valid only if the terminals form an internal port.

Example



Because of the source and the load (2-terminal 1-ports) terminals $\{1,2\}$ and $\{3,4\}$ form internal ports.

Therefore, we can speak of

***'the energy transferred from the source to the load'*.**

Passivity

Definition

Assume KVL and KCL, use $\mathscr{B}_{IP}$. The circuit is $[\![$*passive*$]\!]$ $:\Leftrightarrow [\![$ $(I,P) \in \mathscr{B}_{IP}, t_0 \in \mathbb{R} \Rightarrow \exists K \in \mathbb{R}$ such that

$$-\int_{t_0}^{t} \left(\sum_{k=1}^{N} I_k(t) P_k(t) \right) dt < K \qquad \text{for } t \geq t_0 \,]\!]. \tag{1}$$

Passivity $:\Leftrightarrow$ only finite amount of extractable energy.

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Passivity $:\Leftrightarrow$ only finite amount of extractable energy.

$\mathscr{B}_{IP}$ is passive $\Leftrightarrow \exists\, V : \mathbb{R} \to [0,\infty)$, called a *storage*, such that

$$V(t_2) - V(t_1) \leq \int_{t_1}^{t_2} \left(\sum_{k=1}^{N} I_k(t) P_k(t) \right) dt$$

for $(I,P) \in \mathscr{B}_{IP}$ and $t_1 \geq t_2$.

$\rightsquigarrow$ positive realness, etc.

Concluding remarks

- !! **Use digraphs with leaves instead of graphs** !!

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- **Avoid having to pair terminals as in N-ports.**
- **Avoid dealing with circuits as if the external terminals were driven by current or voltage sources.**

- !! **Use digraphs with leaves instead of graphs** !!
- **Avoid having to pair terminals as in N-ports.**
- **Avoid dealing with circuits as if the external terminals were driven by current or voltage sources.**
- **Note irrelevance and inappropriateness of input/output thinking.**

The lecture frames are available from/at

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Thank you

Thank you

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