PASSIVE SYNTHESIS

of the

TERMINAL BEHAVIOR

of

CIRCUITS

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MTNS 2010, Budapest **July 5, 2010**

Synthesis problem

Informal formulation

Given a system, a *behavior*, and a set of *building blocks*, find an *architecture* and an *embedding* of building blocks such that the interconnected system realizes the given behavior.

We take a look at the following classical case:

- **behavior: a linear time-invariant differential (LTID) current/voltage behavior,**
- **building blocks: linear *passive* resistors, inductors, capacitors, and transformers**
  $\rightsquigarrow$ RLCT synthesis.

Pedigree

Ronald Foster

Wilhelm Cauer

Otto Brune

Raoul Bott & Richard Duffin

Bernard Tellegen

Brockway McMillan

Vitold Belevitch

Sidney Darlington

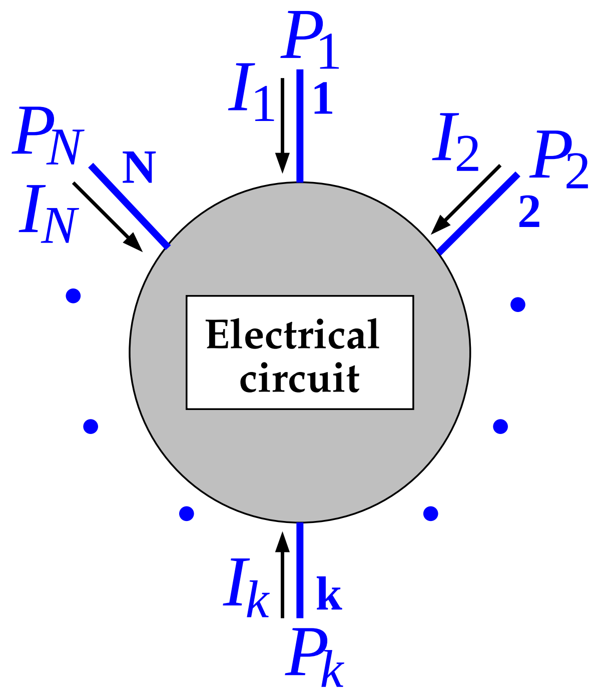
Dante Youla

and many others...

We add some footnotes to the work of these EE pioneers...

N-terminal circuits

Currents and potentials



At each terminal: a current and a potential

$$\rightsquigarrow \Sigma = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B}) \quad \textbf{behavior } \mathscr{B} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$$

$(I_1, I_2, \ldots, I_N, P_1, P_2, \ldots, P_N) : \mathbb{R} \rightarrow \mathbb{R}^N \times \mathbb{R}^N \in \mathscr{B}$ **means:**

this current/potential trajectory is compatible with the circuit architecture and its element values.

Elimination thm. $\rightsquigarrow$ **RLCT circuit $\Rightarrow$ LTID behavior**

Synthesis

For which polynomial matrices $F \in \mathbb{R}[\xi]^{\bullet \times 2N}$ **is**

$$F\left(\frac{d}{dt}\right)\begin{bmatrix} I \\ P \end{bmatrix} = 0$$

the terminal behavior of an RLCT circuit?

!! ***Given such an*** $F \in \mathbb{R}[\xi]^{\bullet \times 2N}$***,***
specify an RLCT circuit that has this terminal behavior **!!**

Further cases of interest:
allow only: RLC, R, RC, RL, LC, RT, etc.

Our two footnotes

- Do we want to realize the *correct behavior*
  or only the *correct controllable part* ?

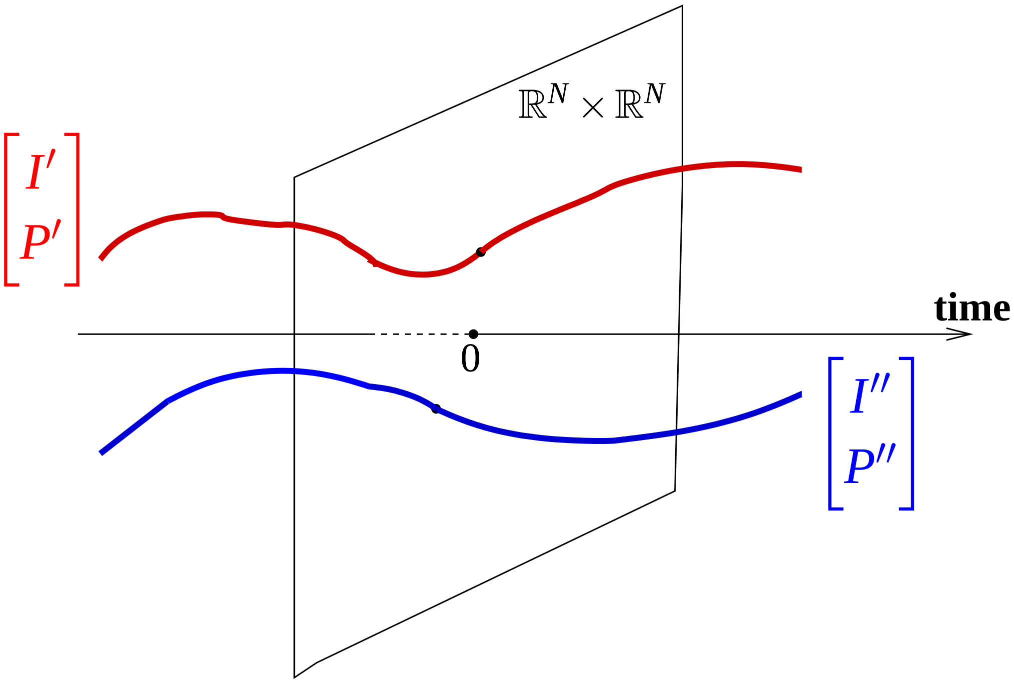
Our two footnotes

- **Do we want to realize the *correct behavior***
  or only the *correct controllable part* ?

- **Do we want to realize an N*-terminal* circuit,**
  or an N*-port* circuit?

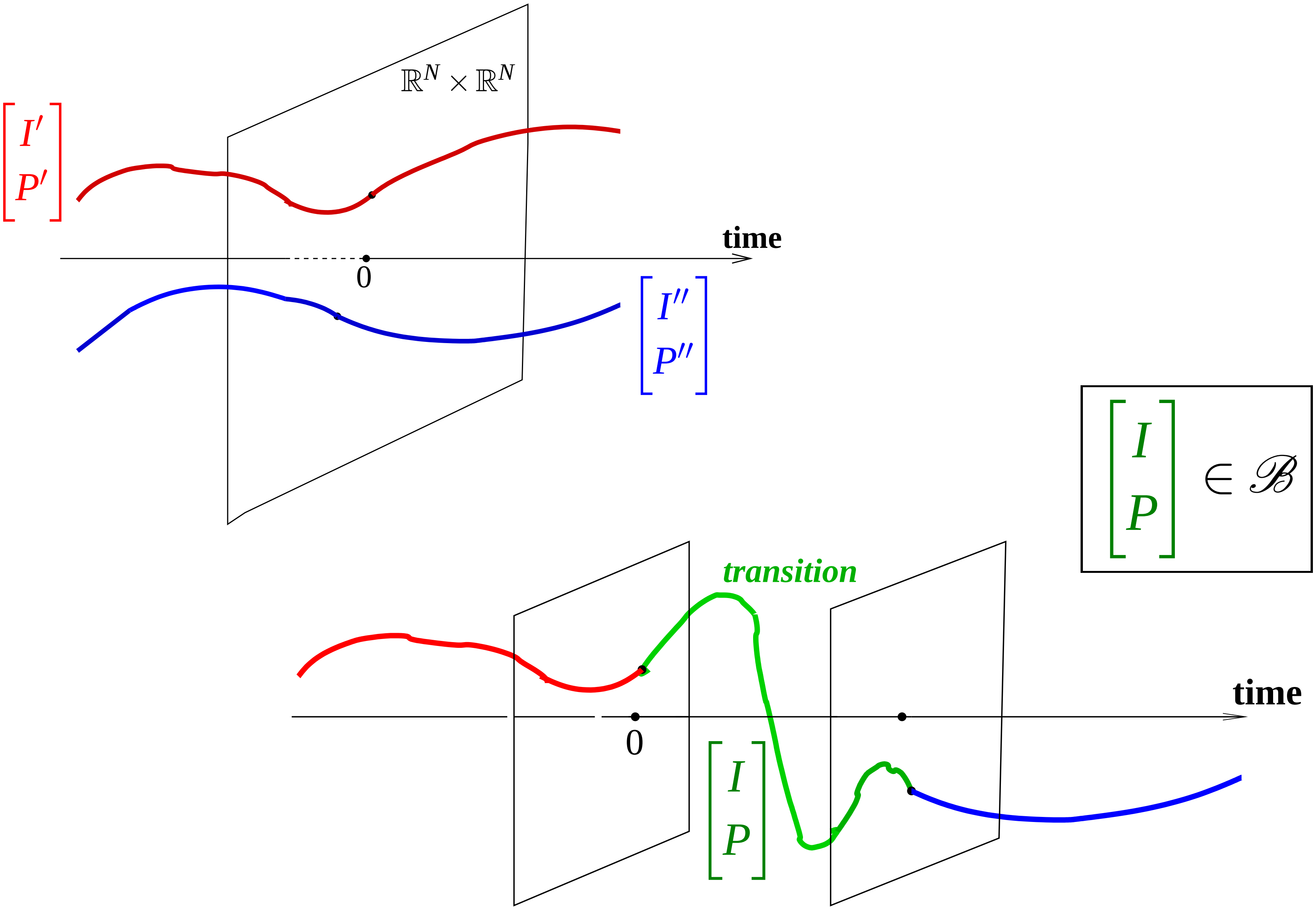
Controllability

Definition of controllability



$$\begin{bmatrix} I' \\ P' \end{bmatrix}, \begin{bmatrix} I'' \\ P'' \end{bmatrix} \in \mathscr{B}$$

Definition of controllability



controllability :⇔ concatenability of trajectories after a delay .

Controllability of LTIDSs

The following are equivalent for $F\left(\frac{d}{dt}\right)\begin{bmatrix} I \\ P \end{bmatrix} = 0$**.**

- $\mathscr{B}$ **is controllable.**
- F **(WLOG full row rank) is left prime.**
- **...**

If $F = LF'$**, with** F' **left prime, then**

$$F'\left(\frac{d}{dt}\right)\begin{bmatrix} I \\ P \end{bmatrix} = 0$$

defines the ***'controllable part'*** **of** $\mathscr{B}$**.**

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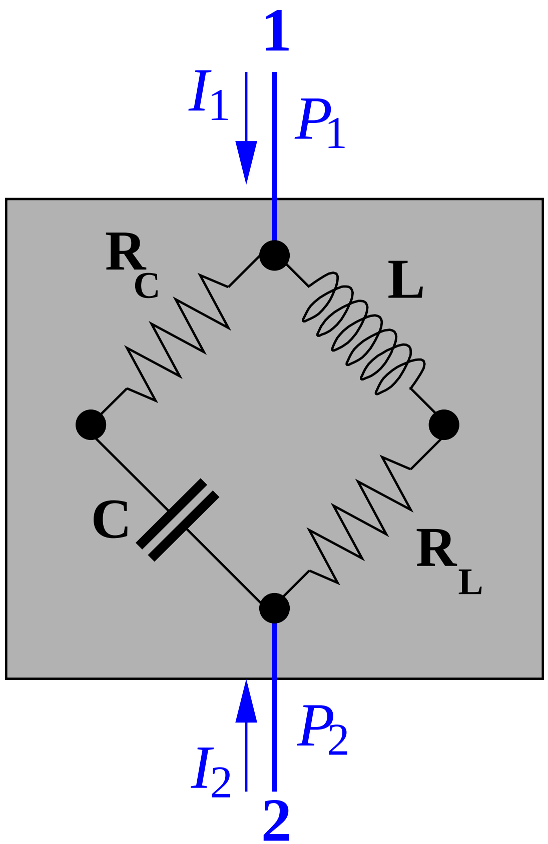
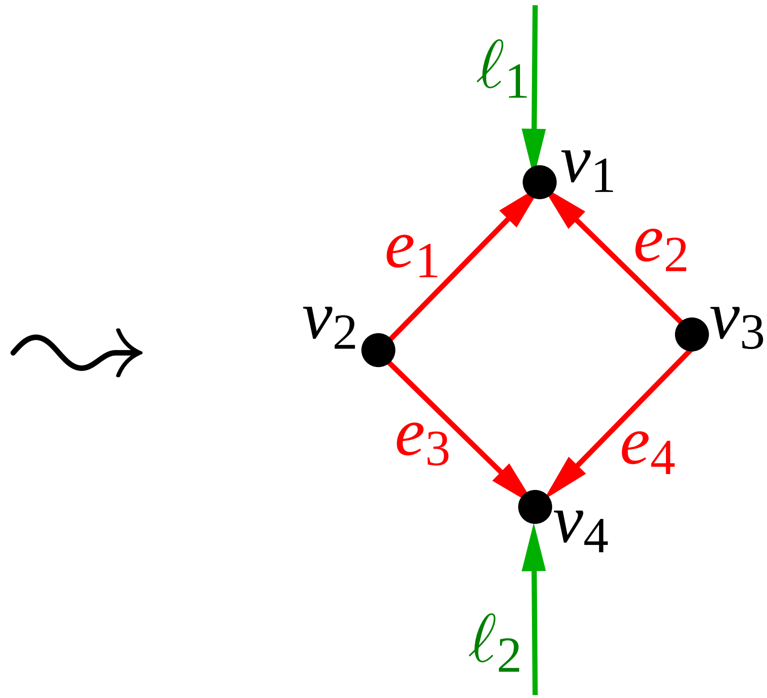
Are uncontrollable circuits degenerate?

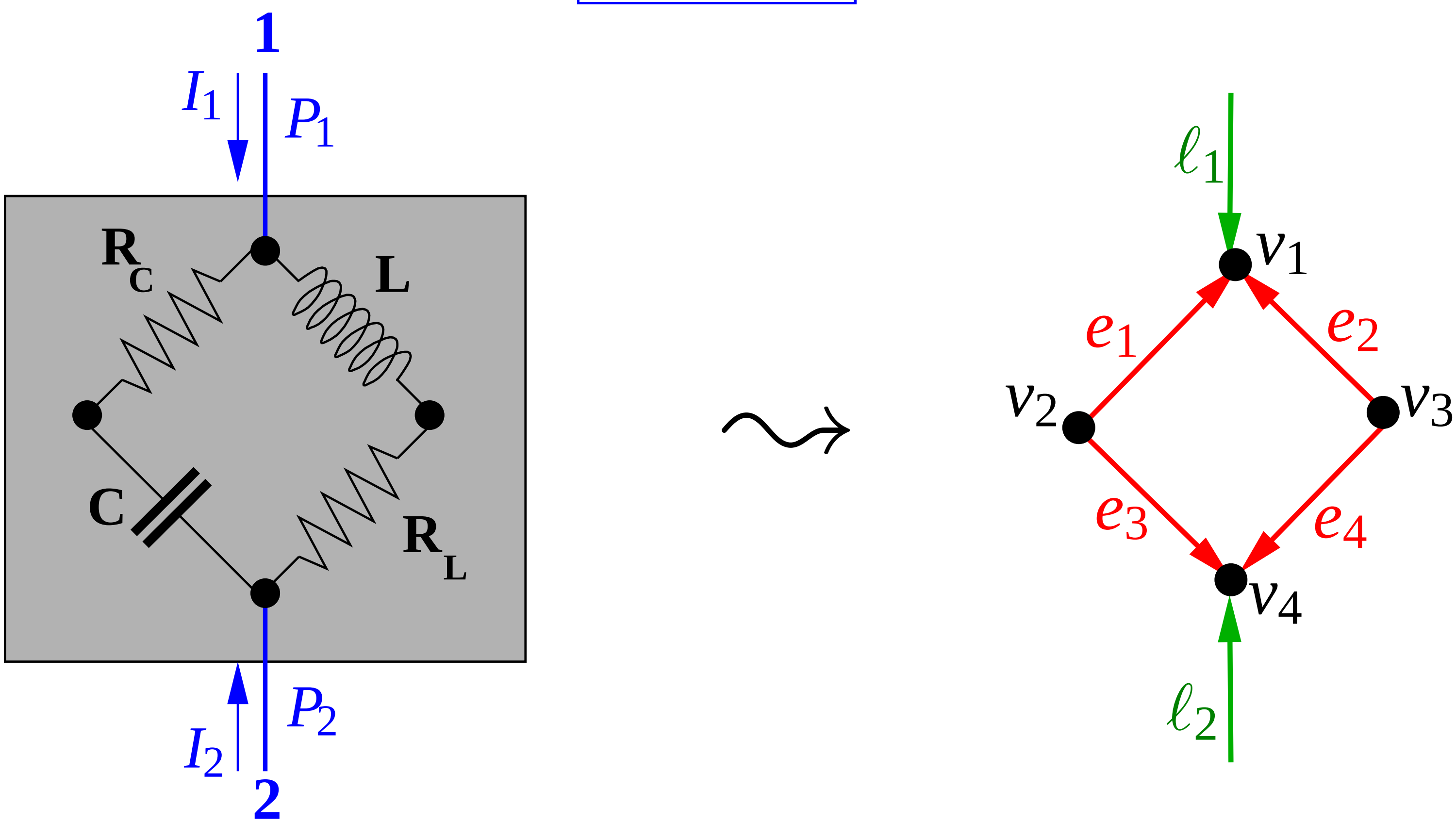
Example





$$\mathbb{A}_{\mathbb{V}} = \begin{bmatrix} +1 & +1 & 0 & 0 \\ -1 & 0 & -1 & 0 \\ 0 & -1 & 0 & -1 \\ 0 & 0 & +1 & +1 \end{bmatrix}, \qquad \mathbb{A}_{\mathbb{L}} = \begin{bmatrix} +1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & +1 \end{bmatrix}.$$

Example



$$I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, P = \begin{bmatrix} P_1 \\ P_2 \end{bmatrix}, \qquad I_{\mathbb{E}} = \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ I_{e_3} \\ I_{e_4} \end{bmatrix}, P_{\mathbb{V}} = \begin{bmatrix} P_{v_1} \\ P_{v_2} \\ P_{v_3} \\ P_{v_4} \end{bmatrix}.$$

Behavioral equations

$$\begin{bmatrix} R_C & 0 & 0 & 0 \\ 0 & L\frac{d}{dt} & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & R_L \end{bmatrix} \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ I_{e_3} \\ I_{e_4} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & C\frac{d}{dt} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} -P_{v_1} + P_{v_2} \\ -P_{v_1} + P_{v_3} \\ P_{v_2} - P_{v_4} \\ P_{v_3} - P_{v_4} \end{bmatrix},$$

$$\begin{bmatrix} I_{e_1} + I_{e_2} + I_1 = 0 \\ I_{e_1} + I_{e_3} = 0 \\ I_{e_2} + I_{e_4} = 0 \\ I_{e_3} + I_{e_4} + I_2 = 0 \end{bmatrix}, \qquad \begin{bmatrix} P_1 = P_{v_1} \\ P_2 = P_{v_4} \end{bmatrix}.$$

Elimination of $I_{\mathbb{E}}$ and $P_{\mathbb{V}} \rightsquigarrow$:

The circuit behavior

$\rightsquigarrow$ **the following ODE defines $\mathscr{B}$.**

Case 1: $CR_C \neq \frac{L}{R_L}$.

$$\left(\frac{R_C}{R_L} + \left(1 + \frac{R_C}{R_L}\right) CR_C \frac{d}{dt} + CR_C \frac{L}{R_L} \frac{d^2}{dt^2}\right) (P_1 - P_2)$$

$$= \left(1 + CR_C \frac{d}{dt}\right) \left(1 + \frac{L}{R_L} \frac{d}{dt}\right) R_C I_1,$$

$$I_1 + I_2 = 0.$$

The circuit behavior

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Case 2: $$CR_C = \frac{L}{R_L}.$$

$$\left(\frac{R_C}{R_L} + CR_C\frac{d}{dt}\right)(P_1 - P_2) = \left(1 + CR_C\frac{d}{dt}\right)R_C\, I_1,$$

$$I_1 + I_2 = 0.$$

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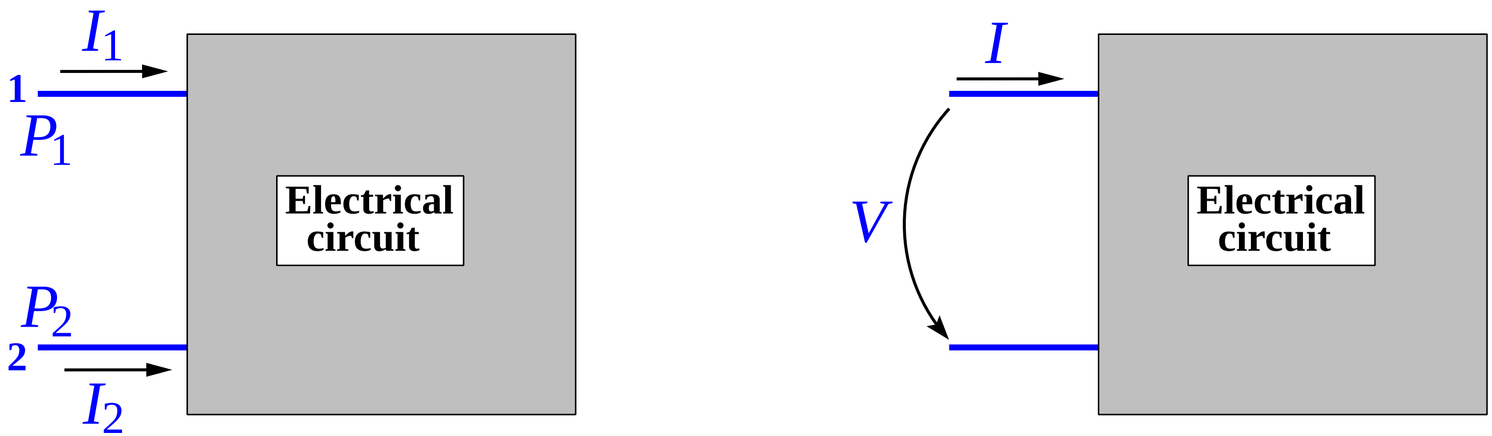
$$I_1 + I_2 = 0.$$

$CR_C = \dfrac{L}{R_L}$ **and** $R_C = R_L \quad \Leftrightarrow \quad$ **uncontrollable.**

Hence: Linear passive circuits can become uncontrollable.

Realization of 2-terminal circuits

2-terminal circuits



KCL $\Rightarrow I_1 + I_2 = 0,$ **KVL** $\Rightarrow$ **only** $P_1 - P_2$ **matters.**

with $I := I_1 = -I_2$ **and** $V := P_1 - P_2$, **this leads to**

$$P\left(\frac{d}{dt}\right) V = Q\left(\frac{d}{dt}\right) I.$$

Define $Z := \frac{Q}{P}$ ***'impedance'*.**

2-terminal circuits

$$P\left(\frac{d}{dt}\right)V = Q\left(\frac{d}{dt}\right)I, \qquad Z = \frac{Q}{P}.$$

Which polynomial pairs (P, Q) are realizable using RLCT? Using RLC?

2-terminal circuits

$$P\left(\frac{d}{dt}\right)V = Q\left(\frac{d}{dt}\right)I, \qquad Z = \frac{Q}{P}.$$

Which polynomial pairs (P, Q) are realizable using RLCT? Using RLC?

Assume P and Q coprime (controllability). Then RLCT realizable iff Z is positive real (Brune).

Iff Z is positive real, then the controllable part is RLCT realizable (Brune).

Iff Z is positive real, then there exists RLC realization with the 'correct' controllable part (Bott-Duffin).

Open problem

Which polynomial pairs (P, Q) are realizable using RLCT?

Necessary condition 1: $Z = \frac{Q}{P}$ **is positive real.**

Necessary condition 2: Uncontrollable part 'stable'.

1 + 2 are not sufficient.

Sufficient condition: P **and** Q **coprime, and** $Z = \frac{Q}{P}$ **p.r.**

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Sufficient condition: P **and** Q **coprime, and** $Z = \dfrac{Q}{P}$ **p.r.**

Conclusions:

The set of RLCT realizable LTID behaviors is unknown.

Bott-Duffin realizes the impedance, but not the behavior.

Example

There is no present theory that guarantees that

$$\left(1+\frac{d}{dt}\right)(P_1 - P_2) = \left(1+\frac{d}{dt}\right) I_1, \qquad I_1 + I_2 = 0$$

is realizable.

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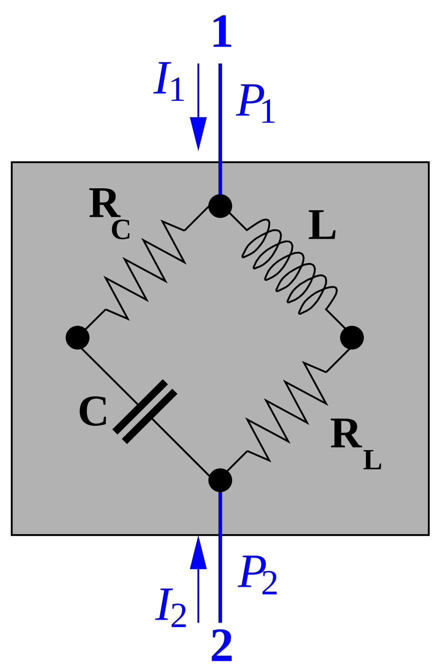
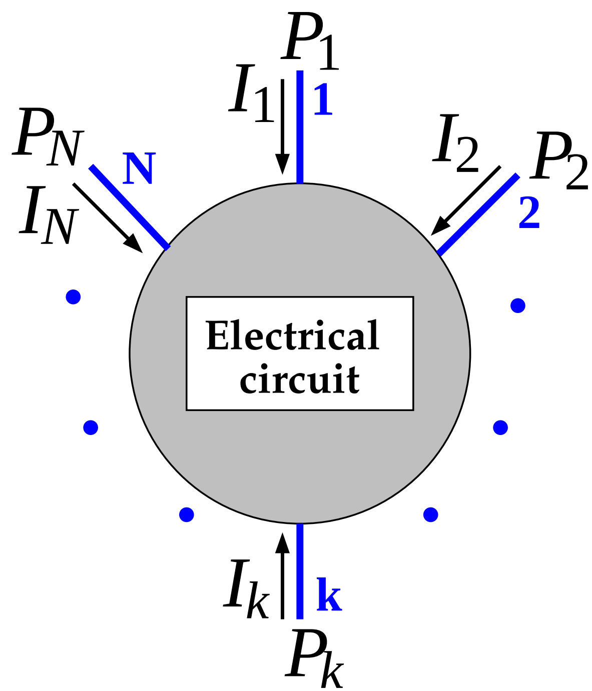
$$\left(1+\frac{d}{dt}\right)(P_1 - P_2) = \left(1+\frac{d}{dt}\right) I_1, \qquad I_1 + I_2 = 0$$

is realizable. It is, using $R_C = R_L = 1, C = 1, L = 1$**.**



N-port versus N-terminal circuits

N-terminal circuit



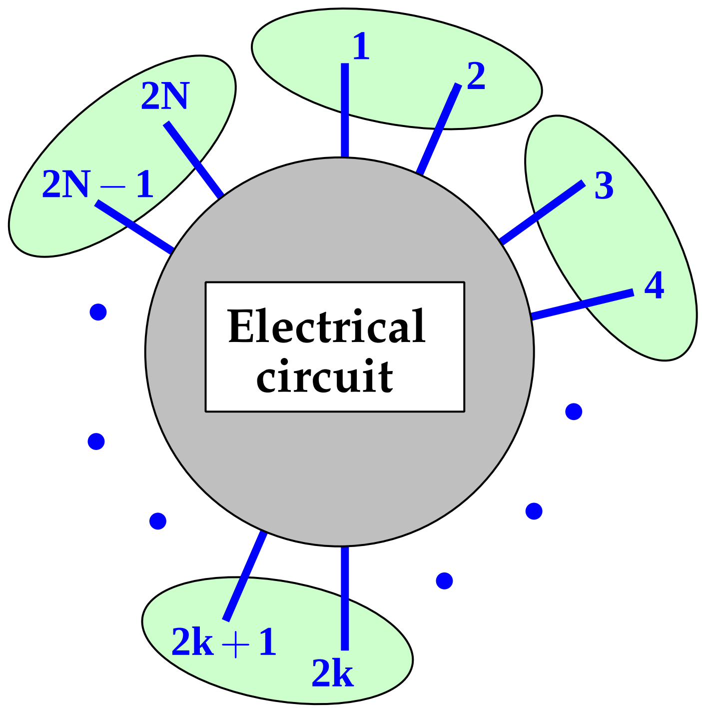
At each terminal: a current and a potential

$\rightsquigarrow \Sigma = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B})$ **behavior** $\mathscr{B} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$

$(I_1, I_2, \ldots, I_N, P_1, P_2, \ldots, P_N) : \mathbb{R} \to \mathbb{R}^N \times \mathbb{R}^N \in \mathscr{B}$ **means:**

this current/potential trajectory is compatible with the circuit architecture and its element values.

N-port



$2N$-terminal circuit
behavior $\mathscr{B} \subseteq \left(\mathbb{R}^{2N} \times \mathbb{R}^{2N}\right)^{\mathbb{R}}$

Pair the terminals, set

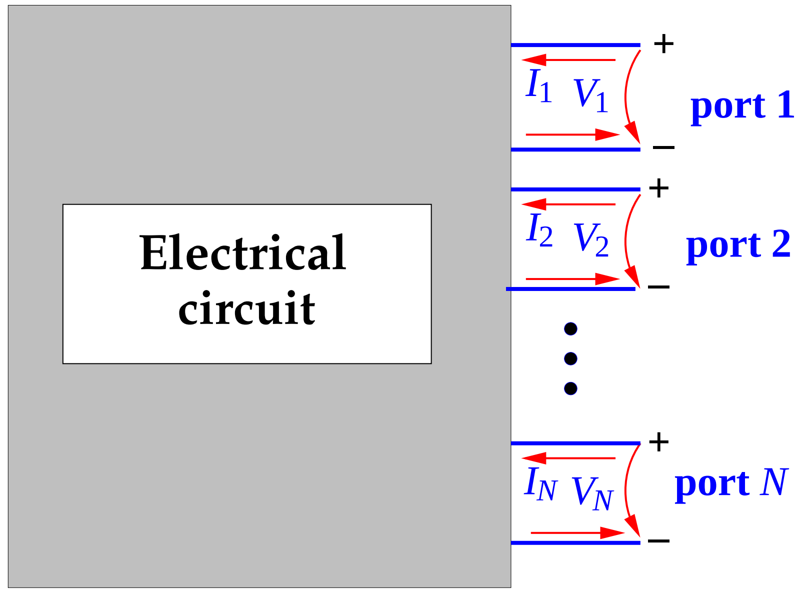
$$\boxed{I_1 + I_2 = 0, \;\; I_3 + I_4 = 0, \cdots, I_{2N-1} + I_{2N} = 0,}$$

and take as variables the *'port' currents* and *'port' voltages*

$$I'_1 = I_1, \;\; I'_2 = I_3, \cdots, I'_N = I_{2N-1},$$

$$V_1 = P_1 - P_2, \;\; V_2 = P_3 - P_4, \cdots, V_N = P_{2N-1} - P_{2N}.$$

Currents and voltages



$$\rightsquigarrow \Sigma = (\mathbb{R}, \mathbb{R}^N \times \mathbb{R}^N, \mathscr{B}) \quad \textbf{port behavior } \mathscr{B} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$$

$(I_1, I_2, \ldots, I_N, V_1, V_2, \ldots, V_N) : \mathbb{R} \to \mathbb{R}^N \times \mathbb{R}^N \in \mathscr{B}$ **means:**

this current/voltage trajectory is compatible with the circuit *and the port current constraints*.

Classical synthesis problem

Given a LTID behavior $\mathscr{B} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$**,**

find a 2N**-terminal RLCT circuit with** N**-port behavior** $\mathscr{B}$**.**

Classical synthesis problem

Given a LTID behavior $\mathscr{B} \subseteq \left(\mathbb{R}^N \times \mathbb{R}^N\right)^{\mathbb{R}}$,
find a 2N-terminal RLCT circuit with N-port behavior $\mathscr{B}$.

- **For the 2-terminal case, KCL and KVL imply that 1-port synthesis is equivalent to 2-terminal synthesis.**
- ***If transformers are allowed* in the synthesis, then the results of the N-port case and the N-terminal case are transferrable.**
  Modulo controllability, a RLCT synthesis exists iff, roughly, the multivariable impedance is symmetric and positive real.
- **Without transformers, the N-port and the N-terminal cases are distinct.**

Resistive terminal synthesis

Transformerless resistive synthesis

The synthesis of resistive N-ports without transformers is one of the open problems of classical N-port synthesis.

For N-terminal synthesis, it can be solved completely.

Realizability

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} Y_{1,1} & Y_{1,2} & \cdots & Y_{1,N} \\ Y_{2,1} & Y_{2,2} & \cdots & Y_{2,N} \\ \vdots & \vdots & \vdots & \vdots \\ Y_{N,1} & Y_{N,2} & \cdots & Y_{N,N} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_N \end{bmatrix}$$

can be realized as an N-terminal circuit using only resistors
if and only if the matrix $Y \in \mathbb{R}^{N \times N}$

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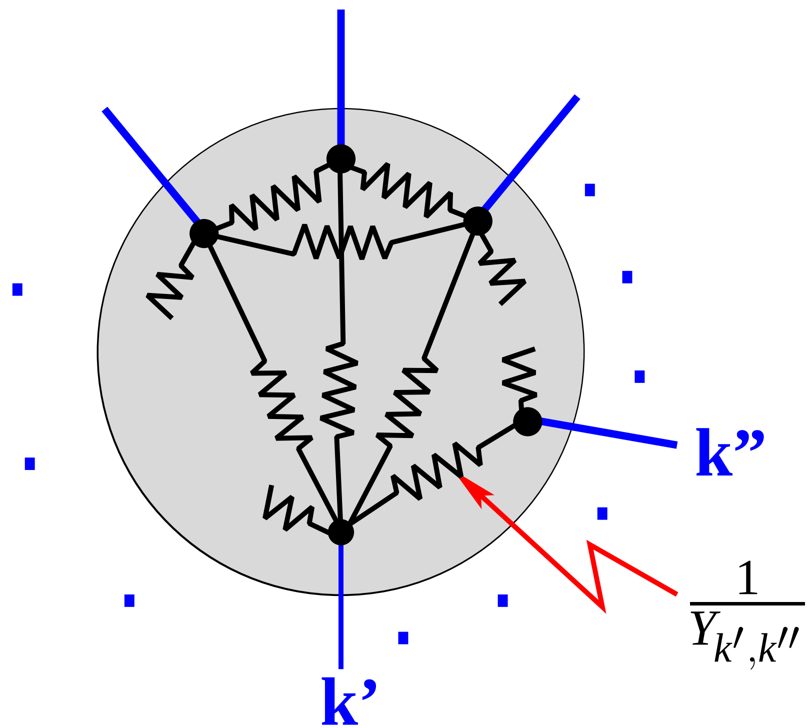
can be realized as an N-terminal circuit using only resistors if and only if the matrix $Y \in \mathbb{R}^{N \times N}$

- **is symmetric,**
- **has diagonal elements ≥ 0,**
- **off-diagonal elements ≤ 0,**
- **and row sums (and hence column sums) $= 0$.**

'hyperdominant with zero excess'.

Terminal synthesis of resistive circuits



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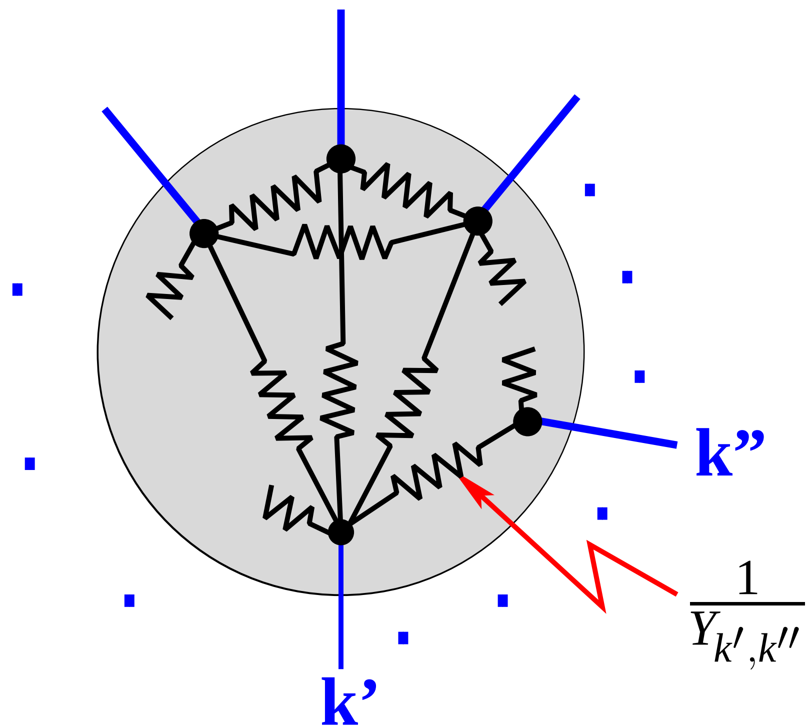

- **Generalizes to not-voltage-controlled case.**

  $\rightsquigarrow$ **realizability using only** R**’s of** $F\begin{bmatrix} I \\ P \end{bmatrix} = 0$**.**

- **Generalizes to inductive and capacitive circuits.**

RLC terminal synthesis

Terminal synthesis of RLC circuits

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} Y_{1,1}\left(\frac{d}{dt}\right) & Y_{1,2}\left(\frac{d}{dt}\right) & \cdots & Y_{1,N}\left(\frac{d}{dt}\right) \\ Y_{2,1}\left(\frac{d}{dt}\right) & Y_{2,2}\left(\frac{d}{dt}\right) & \cdots & Y_{2,N}\left(\frac{d}{dt}\right) \\ \vdots & \vdots & \vdots & \vdots \\ Y_{N,1}\left(\frac{d}{dt}\right) & Y_{N,2}\left(\frac{d}{dt}\right) & \cdots & Y_{N,N}\left(\frac{d}{dt}\right) \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_N \end{bmatrix}$$

can be realized as an N-terminal RLC circuit if $Y \in \mathbb{R}[\xi]^{N\times N}$

- **is symmetric,**
- **has diagonal elements positive real,**
- $-$ **off-diagonal elements positive real,**
- **and row sums (and hence column sums)** $= 0$**.**

Not necessary!

Terminal synthesis of RLC circuits

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} Y_{1,1}\left(\frac{d}{dt}\right) & Y_{1,2}\left(\frac{d}{dt}\right) & \cdots & Y_{1,N}\left(\frac{d}{dt}\right) \\ Y_{2,1}\left(\frac{d}{dt}\right) & Y_{2,2}\left(\frac{d}{dt}\right) & \cdots & Y_{2,N}\left(\frac{d}{dt}\right) \\ \vdots & \vdots & \vdots & \vdots \\ Y_{N,1}\left(\frac{d}{dt}\right) & Y_{N,2}\left(\frac{d}{dt}\right) & \cdots & Y_{N,N}\left(\frac{d}{dt}\right) \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_N \end{bmatrix}$$

can be realized as an N-terminal RLC circuit only if

$Y \in \mathbb{R}[\xi]^{N \times N}$

- **is symmetric,**
- **has diagonal elements $Y_{k',k'}(\lambda) \geq 0$ for $\lambda \in \mathbb{R}, \lambda \geq 0$,**
- **off-diagonal elements $Y_{k',k''}(\lambda) \leq 0$ for $\lambda \in \mathbb{R}, \lambda \geq 0$,**
- **and row sums (and hence column sums) $= 0$.**

Not sufficient!

Holy grail

Bott-Duffin synthesis from terminal point of view!

Conclusions

- **Classical impedance synthesis considers only the controllable part.**
  RLCT synthesis of uncontrollable LTID behaviors is an open problem.

- **Classical impedance synthesis considers only the controllable part.**
  RLCT synthesis of uncontrollable LTID behaviors is an open problem.
- ***N*-terminal synthesis is more natural than the classical *N*-port synthesis question.**
  The resistive *N*-terminal synthesis problem is completely solvable.
  For RLC *N*-terminal synthesis we presented a new necessary condition.

Copies of the lecture frames are available from/at

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http://www.esat.kuleuven.be/∼jwillems

Thank you

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