MODELING INTERCONNECTED SYSTEMS

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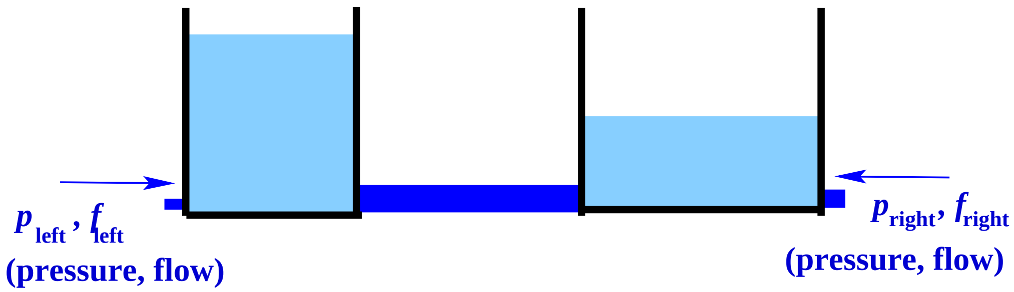
Objective

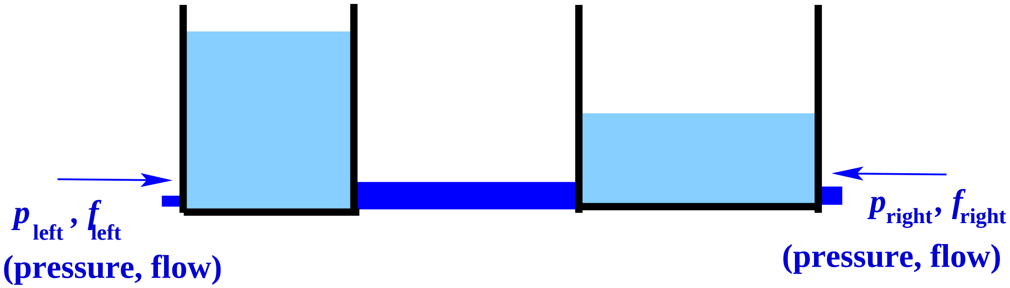
Develop a mathematical framework for dealing with interconnected (open, dynamical) systems.

Competing philosophies:

- **input/output signal flow graphs**
- **circuit diagrams**
- **bond graphs**
- **object-oriented modeling (SPICE, Modelica, ...)**
- **...**

A simple example


p left , f left
(pressure, flow)
p right, f right
(pressure, flow)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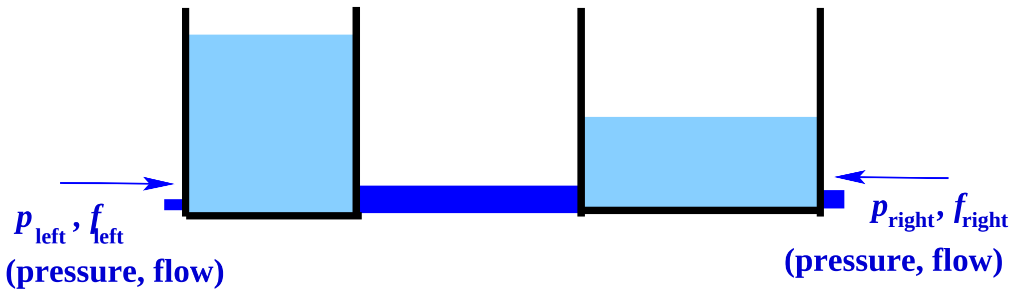
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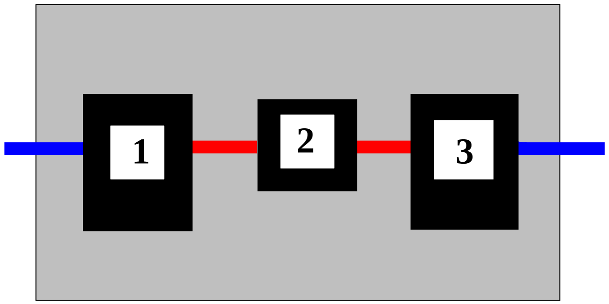
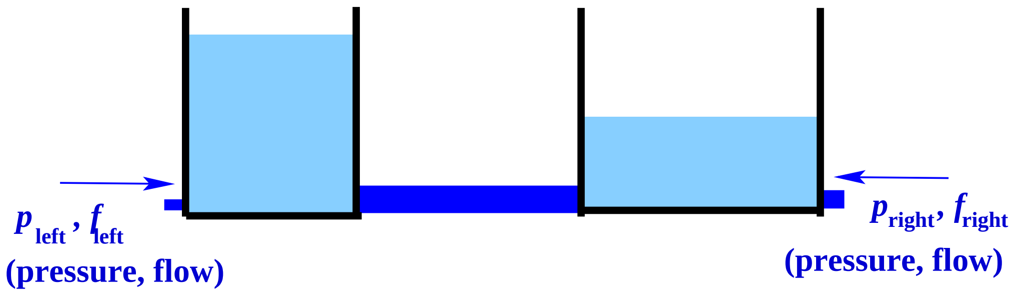

1
2
3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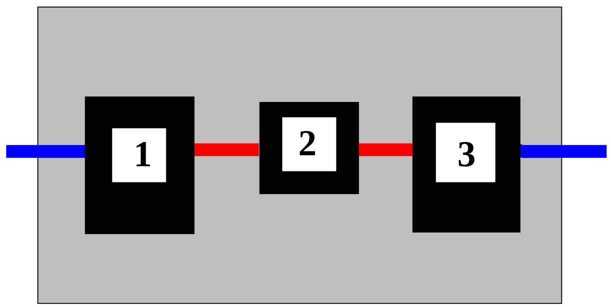
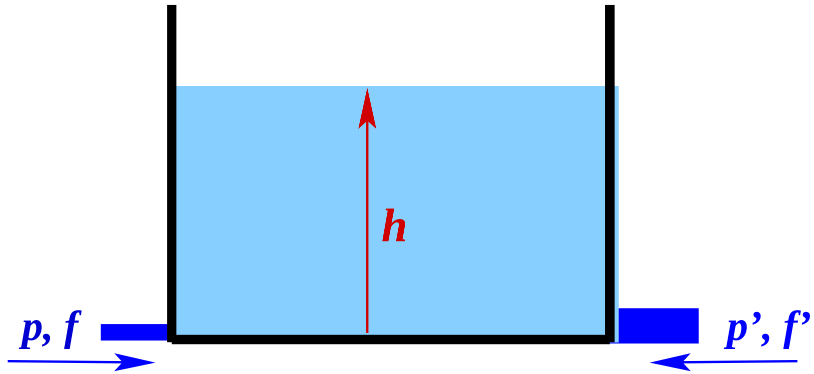
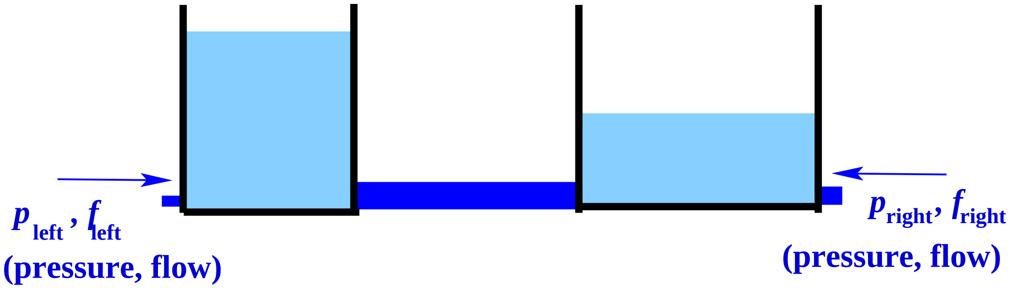
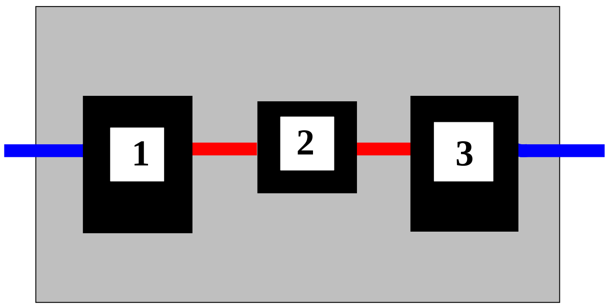

1
2
3

black box 1 & 3:


h
p, f
p’, f’





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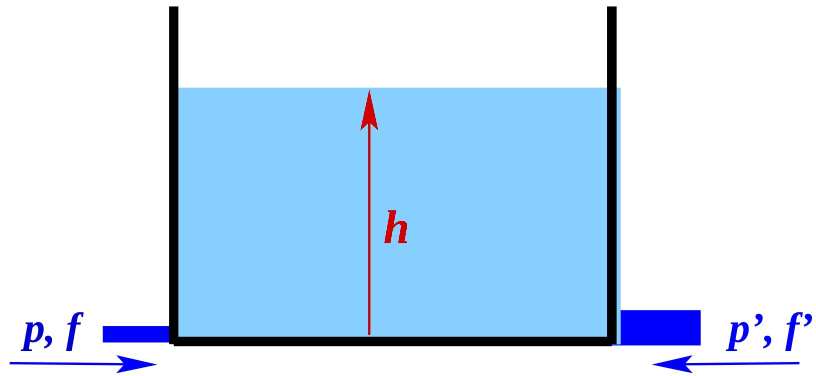
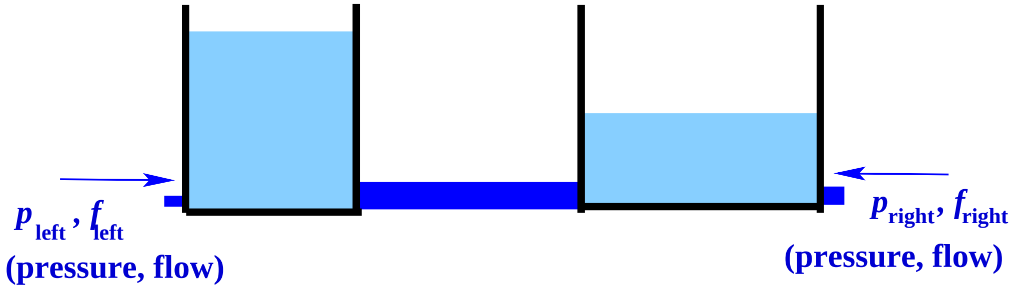
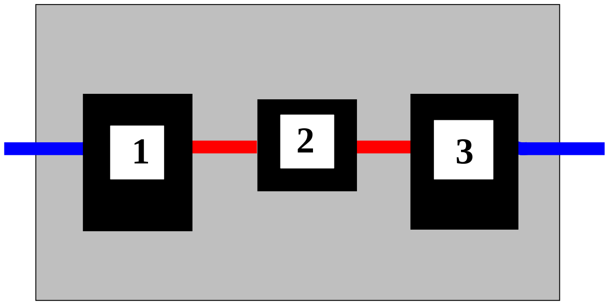


black box 2:





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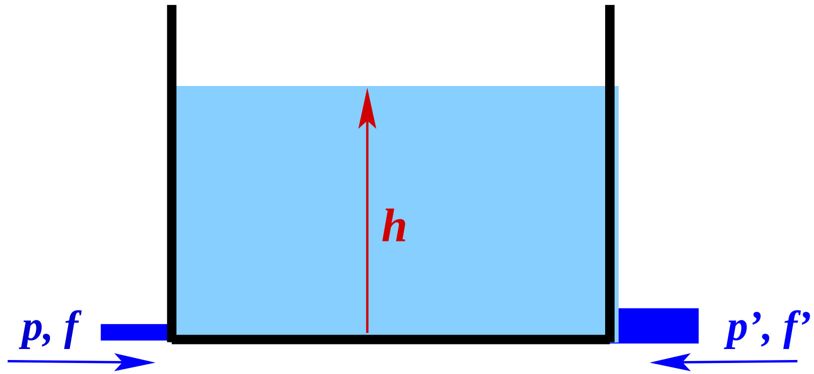
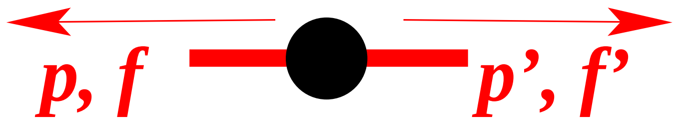


black box 2:

interconnections:



Black box 1:

$$A_1 \frac{d}{dt} h_1 = f_1 + f_1'$$

$$B_1 f_1 = \begin{cases} \sqrt{|p_1 - p_0 - \rho h_1|} & \text{if } p_1 - p_0 \geq \rho h_1 \\ -\sqrt{|p_1 - p_0 - \rho h_1|} & \text{if } p_1 - p_0 \leq \rho h_1 \end{cases}$$

$$C f_1' = \begin{cases} \sqrt{|p_1' - p_0 - \rho h_1|} & \text{if } p_1' - p_0 \geq \rho h_1 \\ -\sqrt{|p_1' - p_0 - \rho h_1|} & \text{if } p_1' - p_0 \leq \rho h_1 \end{cases}$$

Black box 2:

$$f_2 = -f_2', \quad p_2 - p_2' = \alpha f_2$$

Black box 3:

$$A_3 \frac{d}{dt} h_3 = f_3 + f_3'$$

$$C f_3 = \begin{cases} \sqrt{|p_3 - p_0 - \rho h_3|} & \text{if } p_3 - p_0 \geq \rho h_3 \\ -\sqrt{|p_3 - p_0 - \rho h_3|} & \text{if } p_3 - p_0 \leq \rho h_3 \end{cases}$$

$$C_3 f_3' = \begin{cases} \sqrt{|p_3' - p_0 - \rho h_3|} & \text{if } p_3' - p_0 \geq \rho h_3 \\ -\sqrt{|p_3' - p_0 - \rho h_3|} & \text{if } p_3' - p_0 \leq \rho h_3 \end{cases}$$

Interconnection laws:

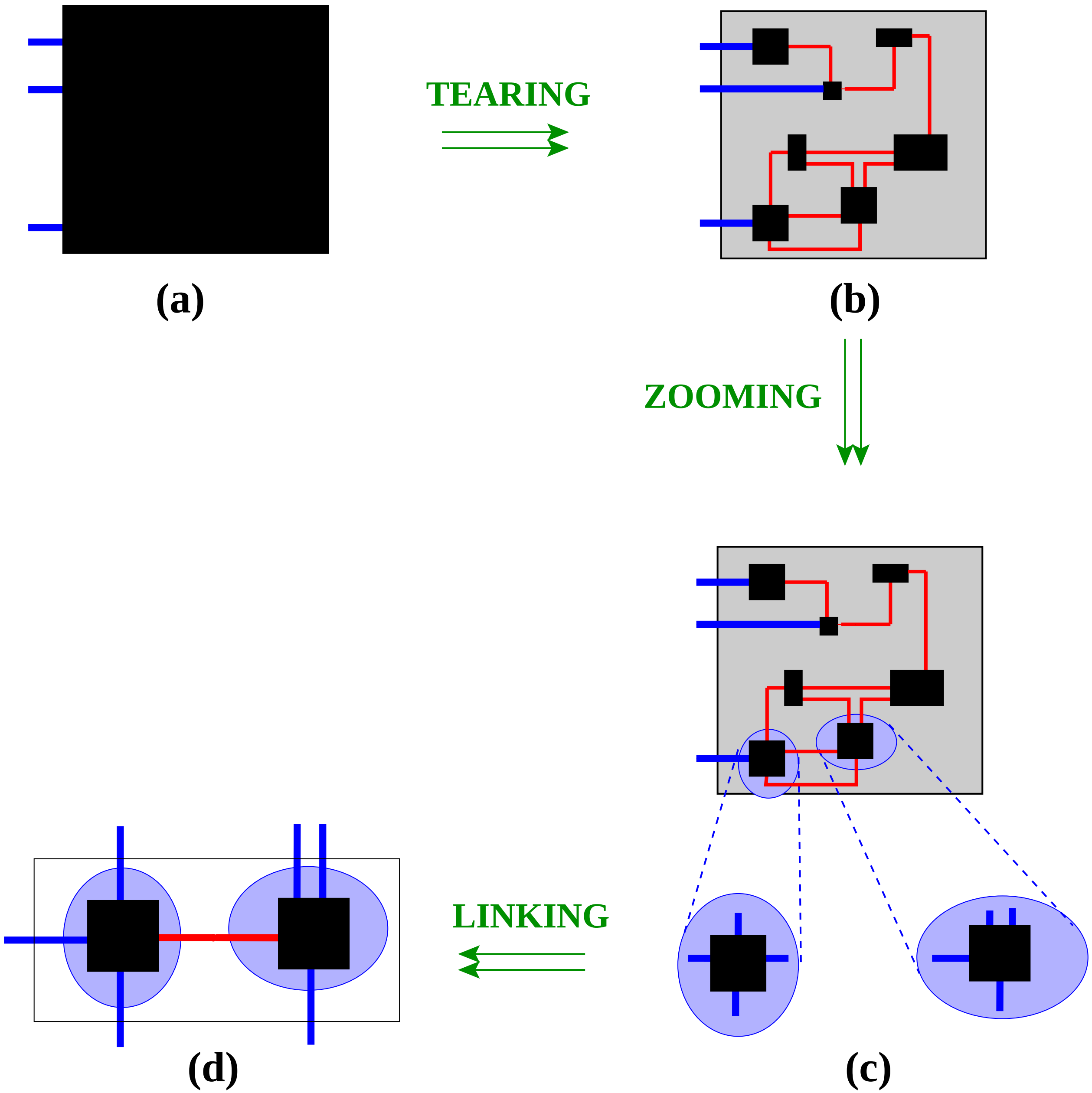
$$p_1' = p_2, \ f_1' + f_2 = 0, \ p_2' = p_3, \ f_2' + f_3 = 0$$

Variables of interest:

$$p_{\text{left}} = p_1, \ f_{\text{left}} = f_1, \ p_{\text{right}} = p_3', \ f_{\text{right}} = f_3'$$

Formalization

Idea



Tearing, zooming, linking language

(i) terminals

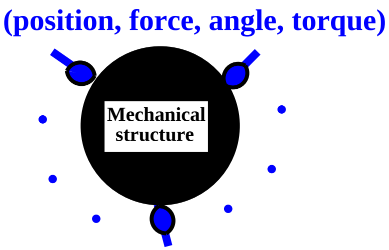
(ii) (parameterized) modules

(iii) the interconnection architecture

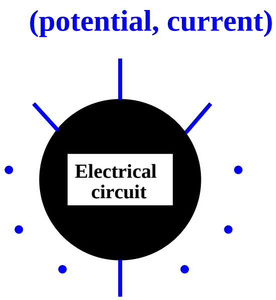
(iv) the module embedding

(v) the manifest variable assignment

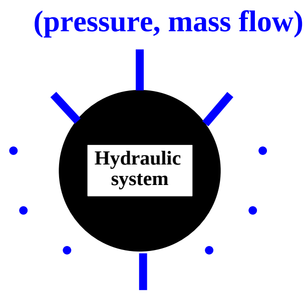
Terminals and Modules



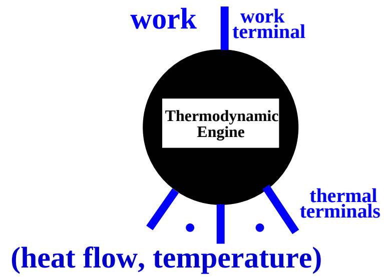
(a)



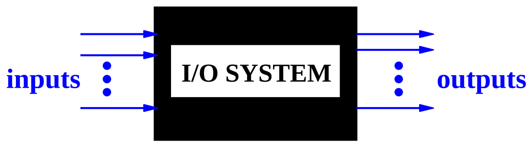
(b)



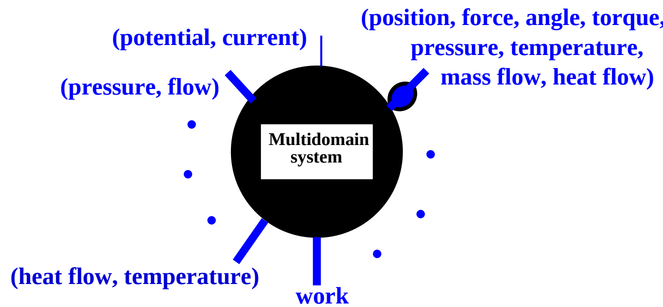
(c)



(d)

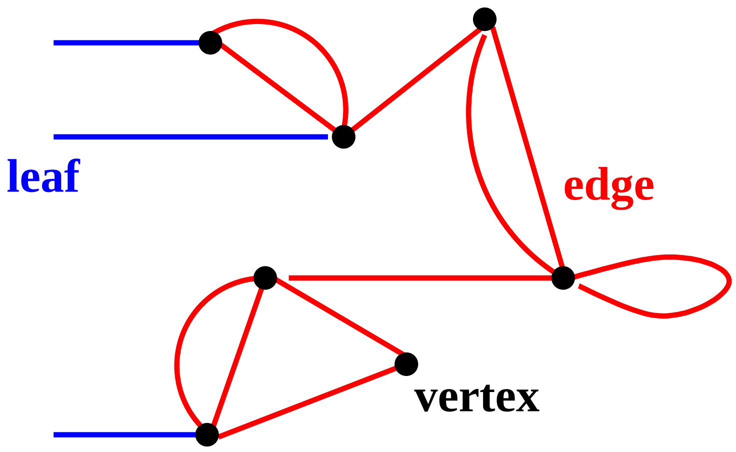


(e)

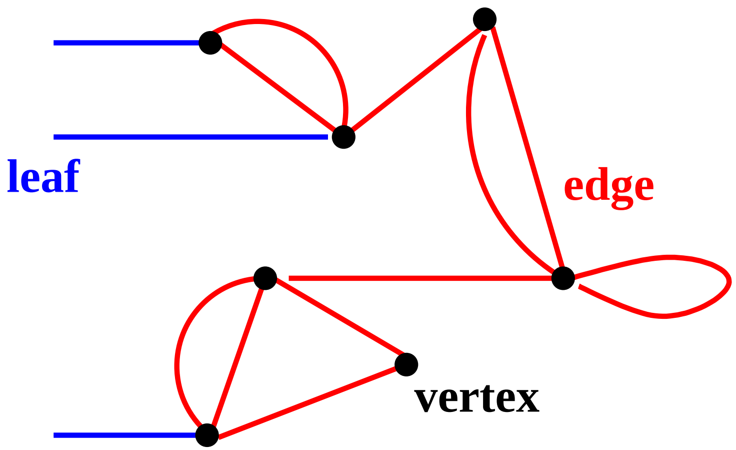


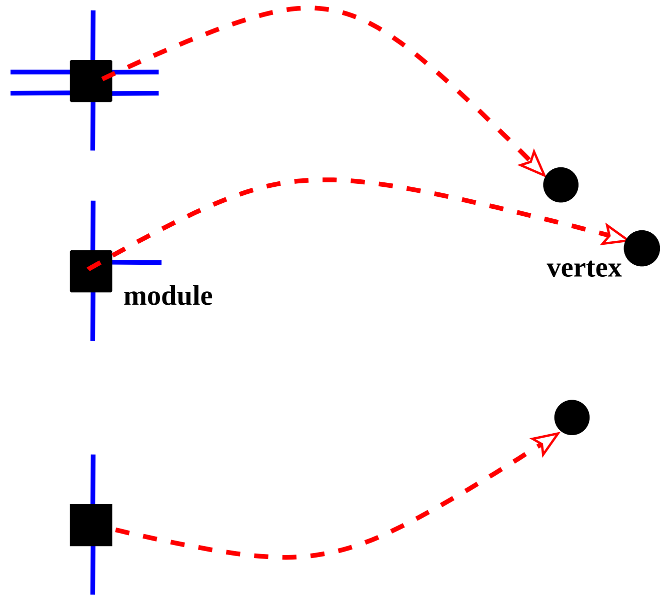
(f)

Architecture & module embedding

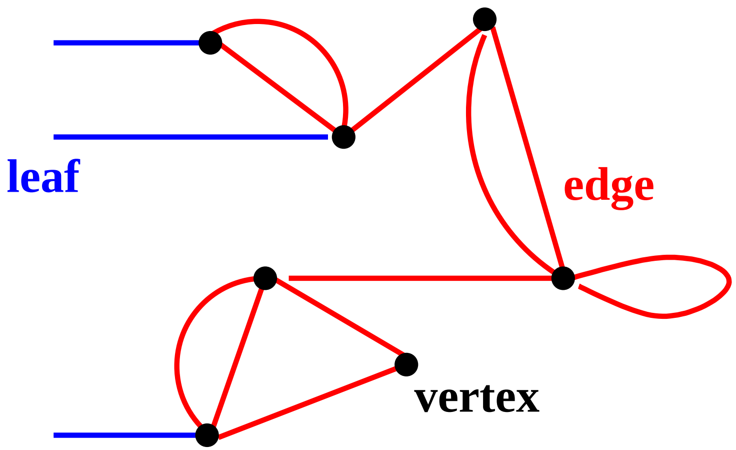


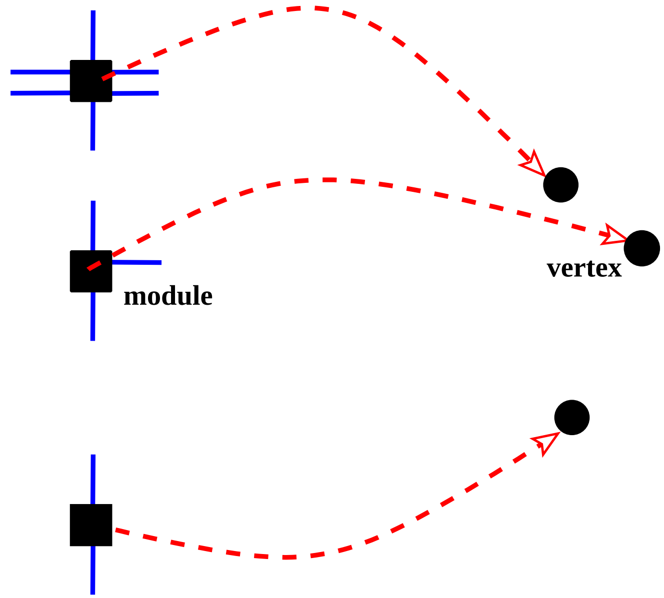
Architecture & module embedding

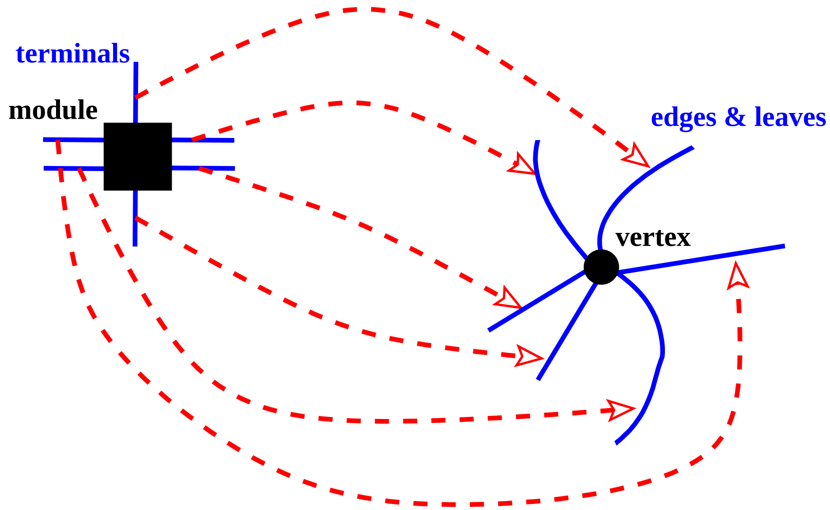




Architecture & module embedding







Interconnection architecture

A ***graph with leaves*** **defined as** $\mathcal{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, \mathcal{A})$

- $\mathbb{V}$ **the set of** ***vertices*****,**
- $\mathbb{E}$ **the set of** ***edges*****,**
- $\mathbb{L}$ **the set of** ***leaves*****,**
- $\mathcal{A}$ **the** ***adjacency map*****.**

$\mathcal{A}$ **associates**

with each edge $e \in \mathbb{E}$ **an unordered pair**

$$\mathcal{A}(e) = [v_1, v_2] \quad v_1, v_2 \in \mathbb{V},$$

with each leaf $\ell \in \mathbb{L}$ **an element** $\mathcal{A}(\ell) = v \in \mathbb{V}$**.**

Module embedding

The *module embedding* associates

a module with each vertex,

a $1 \leftrightarrow 1$ assignment between the

edges and leaves adjacent to the vertex and

the terminals of the module.

The edges specify how

terminals of subsystems are connected,

the leaves specify

the interaction with the environment.

Module embedding

Vertices $\rightsquigarrow$ Subsystems

Edges $\rightsquigarrow$ Interconnections

Manifest variables

The *manifest variable assignment* is a map that assigns the manifest variables as a function of the terminal variables.

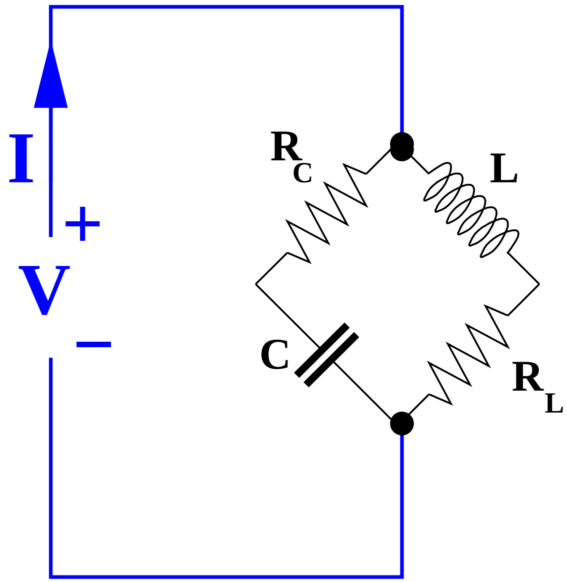
The terminal variables are henceforth considered as latent variables.

Behavioral equations

1. **Module equations for each vertex**
2. **Interconnection constraints for each edge**
3. **Manifest variable assignment**

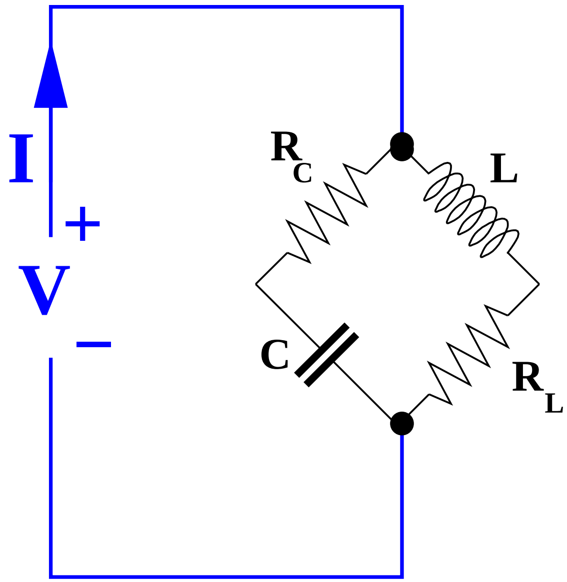
Example

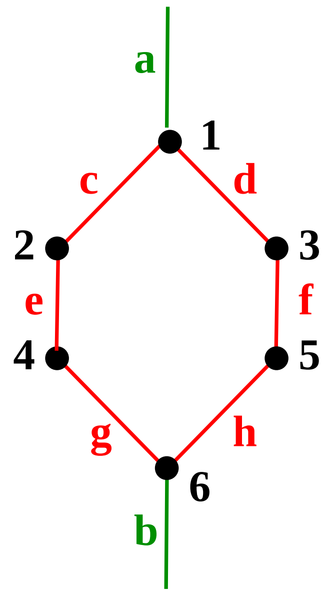
Example



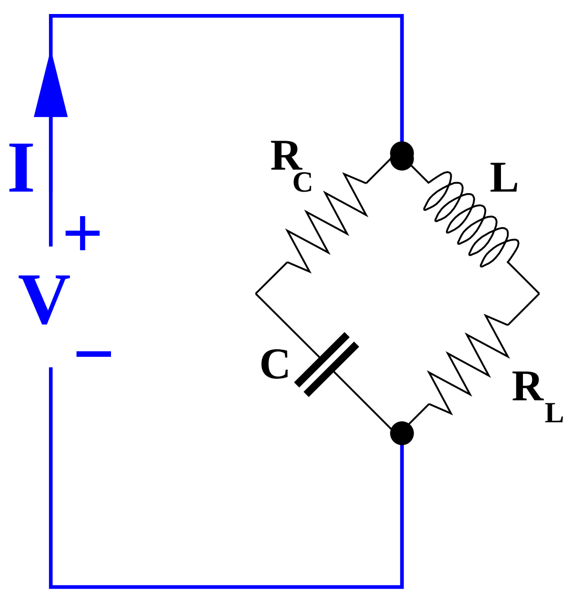
¡¡¡ Model the port behavior !!!

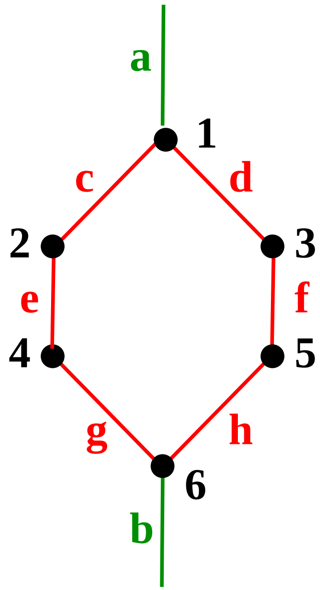
Example





Example





$$R_C \mapsto 2, R_L \mapsto 5, C \mapsto 4, L \mapsto 3, \text{connector}_1 \mapsto 1, \text{connector}_2 \mapsto 6,$$

$$1_{R_C} \mapsto c, 2_{R_C} \mapsto e, 1_{R_L} \mapsto f, 2_{R_L} \mapsto h, 1_C \mapsto e, 2_C \mapsto g, 1_L \mapsto d, 2_L \mapsto f,$$

$$1_{connector_1} \mapsto a, 2_{connector_1} \mapsto c, 3_{connector_1} \mapsto d,$$

$$1_{connector_2} \mapsto b, 2_{connector_2} \mapsto g, 3_{connector_2} \mapsto h.$$

Module equations

vertex 1 : $V_{1_{\text{connector}_1}} = V_{2_{\text{connector}_1}} = V_{3_{\text{connector}_1}},$

$I_{1_{\text{connector}_1}} + I_{2_{\text{connector}_1}} + I_{3_{\text{connector}_1}} = 0;$

vertex 2 : $V_{1_{R_C}} - V_{2_{R_C}} = R_C I_{1_{R_C}},\ I_{1_{R_C}} + I_{2_{R_C}} = 0;$

vertex 3 : $L\frac{d}{dt} I_{I_L} = V_{1_L} - V_{2_L},\ I_{1_L} + I_{2_L} = 0;$

vertex 4 : $C\frac{d}{dt}\left(V_{1_C} - V_{2_C}\right) = I_{1_C},\ I_{1_C} + I_{2_C} = 0;$

vertex 5 : $V_{1_{R_L}} - V_{2_{R_L}} = R_L I_{1_{R_L}},\ I_{1_{R_L}} + I_{2_{R_L}} = 0;$

vertex 6 : $V_{1_{\text{connector}_2}} = V_{2_{\text{connector}_2}} = V_{3_{\text{connector}_2}},$

$I_{1_{\text{connector}_2}} + I_{2_{\text{connector}_2}} + I_{3_{\text{connector}_2}} = 0.$

Interconnection equations

edge c : $V_{1_{R_C}} = V_{2_{\text{connector}_1}},\ I_{1_{R_C}} + I_{2_{\text{connector}_1}} = 0;$

edge d : $V_{1_L} = V_{3_{\text{connector}_1}},\ I_{1_L} + I_{3_{\text{connector}_1}} = 0;$

edge e : $V_{2_{R_C}} = V_{1_C},\ I_{2_{R_C}} + I_{1_C} = 0;$

edge f : $V_{2_L} = V_{1_{R_C}},\ I_{2_L} + I_{1_{R_C}} = 0;$

edge g : $V_{2_C} = V_{1_{\text{connector}_2}},\ I_{2_C} + I_{1_{\text{connector}_2}} = 0;$

edge h : $V_{2_{R_L}} = V_{2_{\text{connector}_2}},\ I_{2_{R_L}} + I_{2_{\text{connector}_2}} = 0.$

Manifest variable assignment

$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

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$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

The module equations

+ the interconnection constraints

+ the manifest variable assignment

form the complete model for

$$V_{\text{external port}}, I_{\text{external port}}$$

Prevalence of latent variables $\rightsquigarrow$ elimination theory.

Manifest behavior

$$\rightsquigarrow \qquad \Sigma = (\mathbb{R}, \mathbb{R}^2, \mathfrak{B})$$

behavior $\mathfrak{B}$ specified by:

Case 1: $CR_C \neq \frac{L}{R_L}$

$$\left(\frac{R_C}{R_L} + \left(1 + \frac{R_C}{R_L}\right) CR_C \frac{d}{dt} + CR_C \frac{L}{R_L} \frac{d^2}{dt^2}\right) V = \left(1 + CR_C \frac{d}{dt}\right) \left(1 + \frac{L}{R_L} \frac{d}{dt}\right) R_C$$

Case 2: $CR_C = \frac{L}{R_L}$

$$\left(\frac{R_C}{R_L} + CR_C \frac{d}{dt}\right) V = (1 + CR_C) \frac{d}{dt} R_C I$$

$\rightsquigarrow$ **behavior: solutions $(V, I) : \mathbb{R} \longrightarrow \mathbb{R}^2$**

Other methodologies

- **Awkwardness of input/output thinking is obvious in both examples**

"Block diagrams unsuitable for serious physical modeling
- the control/physics barrier"

"Behavior based (declarative) modeling is a good alternative"

from K.J. Åström, ***Present Developments in Control Applications***

IFAC 50-th Anniversary Celebration
Heidelberg, September 12, 2006.

Other methodologies

- **Bondgraphs:**
  1. **Mechanical interconnections equate positions, not velocities**
  2. **Not all interconnections involve equating energy transfer**
  3. **Terminals are for interconnection, ports are for energy transfer**

Other methodologies

-
- Circuit diagrams are only good for 2-terminal one-ports. Not ‘closed’ under composition.

SUMMARY

- **Modeling by physical systems proceeds by tearing, zooming, and linking**
- **Hierarchical procedure**

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- **Hierarchical procedure**
- **Importance of latent variables and the** **elimination theorem**

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- **Modeling by physical systems proceeds by tearing, zooming, and linking**
- **Hierarchical procedure**
- **Importance of latent variables and the elimination theorem**
- **Irrelevance of input/output structure**

Reference: Jan C. Willems

The behavioral approach to open and interconnected systems

***Control Systems Magazine*, volume 27, pages 46 – 99, 2007**

Details & copies of the lecture frames are available from/at

`Jan.Willems@esat.kuleuven.be`

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