



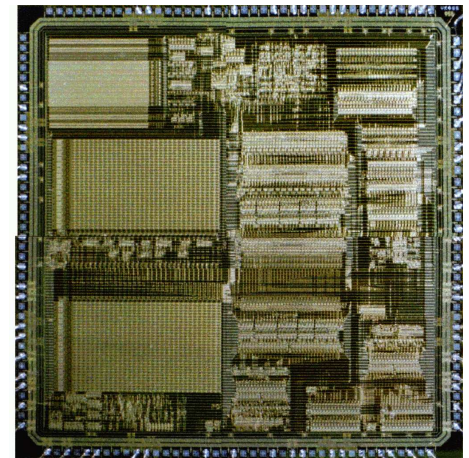
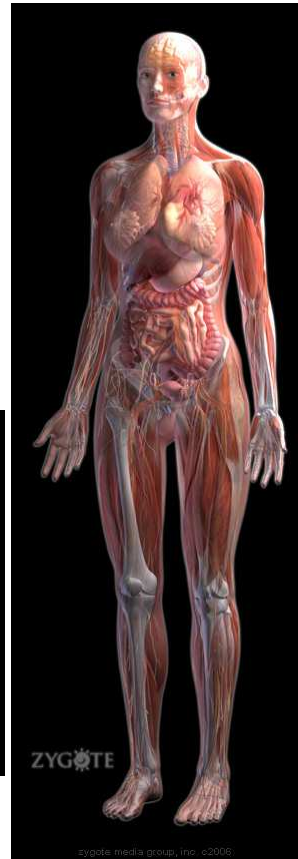
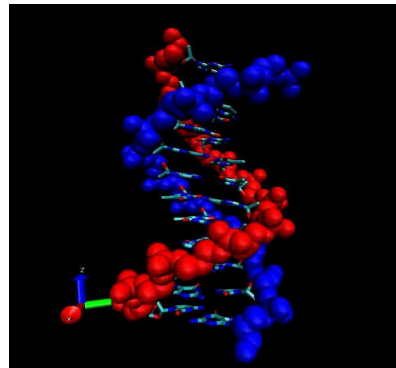
# INTERCONNECTED SYSTEMS

**Jan Willems, K.U. Leuven, Flanders, Belgium**

**Seminar, Kyoto University**

**July 22, 2008**

# Systems



# Features

- **open**
- **interconnected**
- **modular**
- **dynamic**

# Features

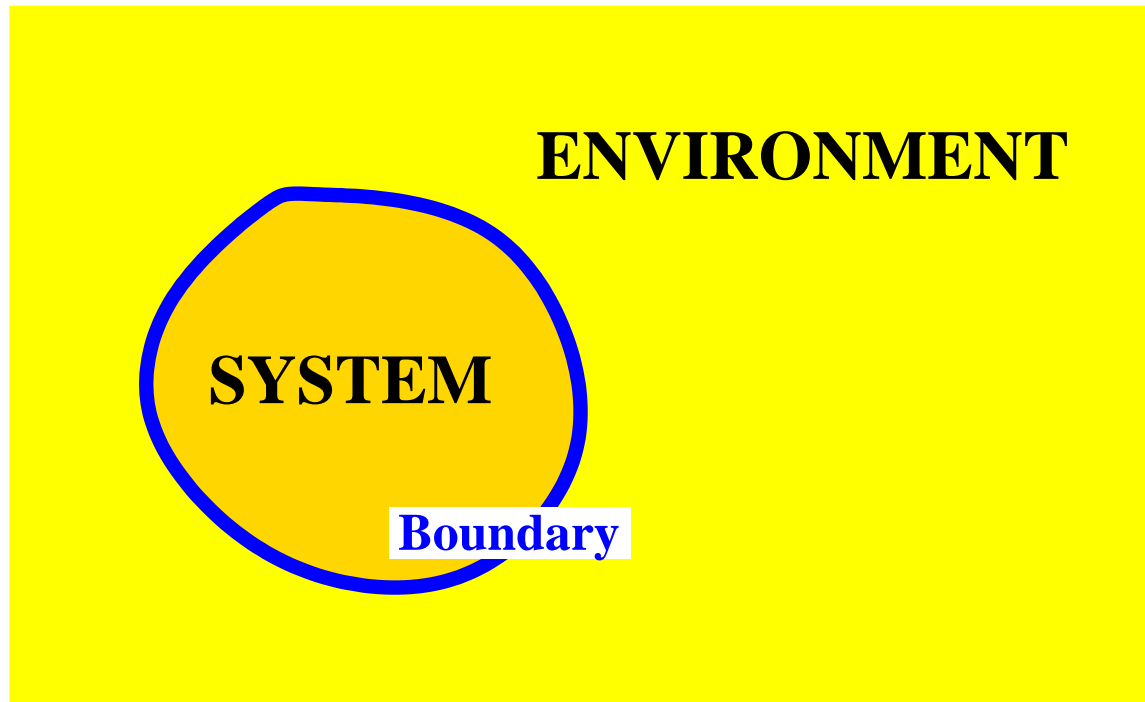
- **open**
- **interconnected**
- **modular**
- **dynamic**

**Theme of this seminar:**

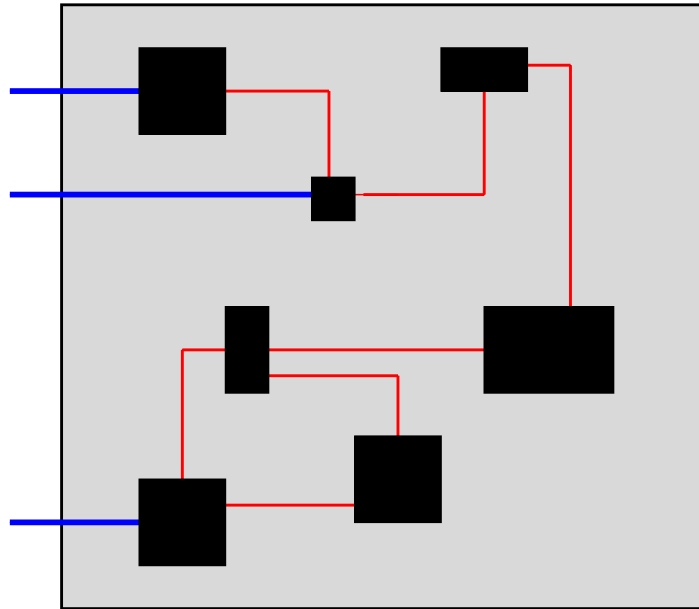
**develop a suitable mathematical framework**

# Open and Connected

**Open**



# Connected

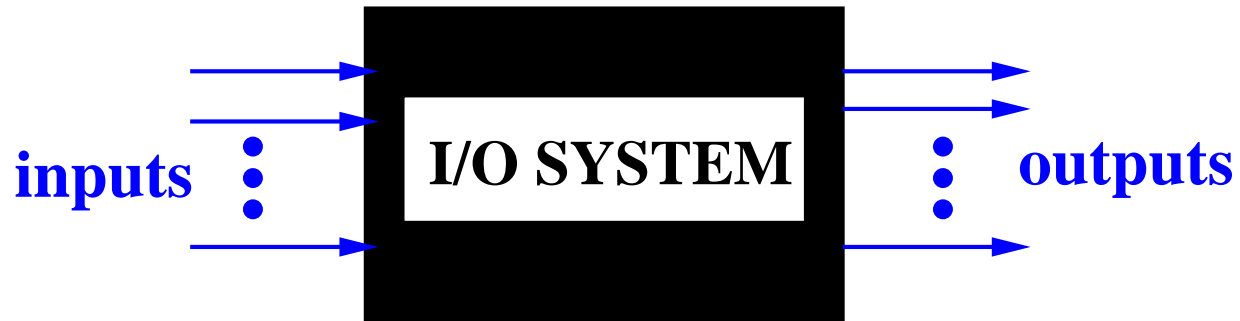
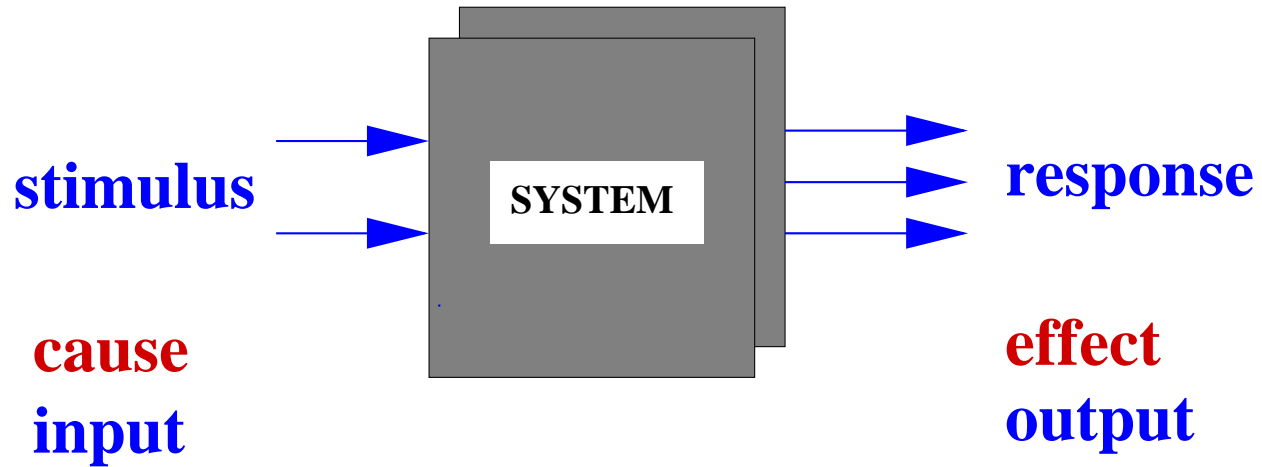


**Architecture with subsystems**

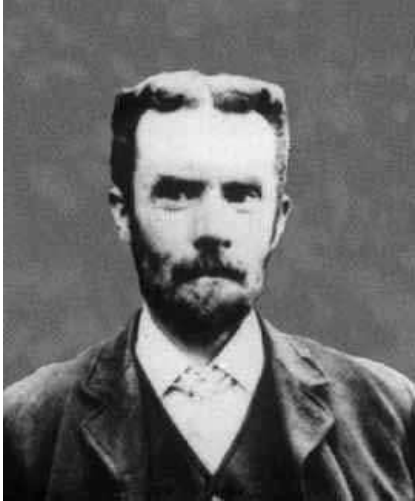


# Inputs and outputs

# Input/output systems



## The originators



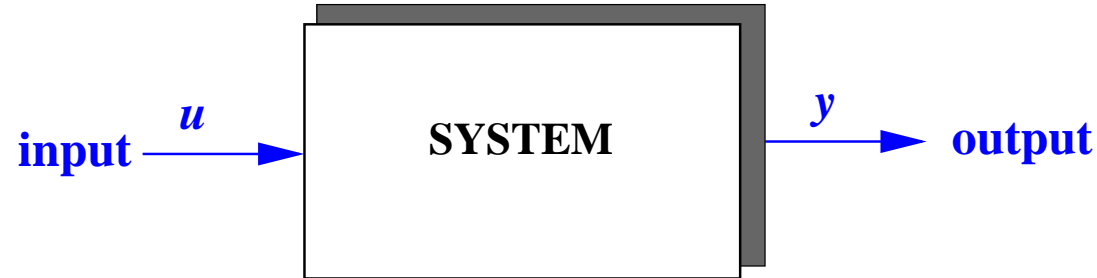
**Oliver Heaviside (1850-1925)**



**Norbert Wiener (1894-1964)**

**and the many electrical circuit theorists ...**

## Mathematical description

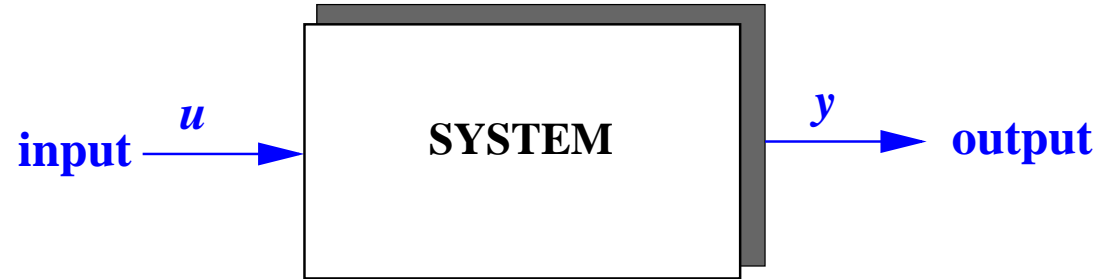


$u$ : input,  $y$ : output,  $p$  and  $q$  polynomials

$G(s) = \frac{q(s)}{p(s)}$  transfer functions, impedances, admittances.

**PID rules. Bode, Nyquist, Nichols. Lead-lag. Root-locus.**

## Mathematical description

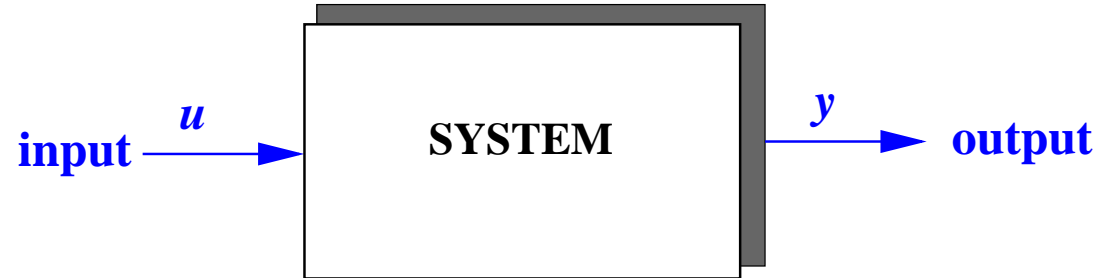


$$y(t) = \int_{0 \text{ or } -\infty}^t H(t-t')u(t') dt'$$

$$y(t) = H_0(t) + \int_{-\infty}^t H_1(t-t')u(t') dt' +$$

$$\int_{-\infty}^t \int_{-\infty}^{t'} H_2(t-t', t'-t'')u(t')u(t'') dt' dt'' + \dots$$

## Mathematical description



$$y(t) = \int_{0 \text{ or } -\infty}^t H(t - t') u(t') dt'$$

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$$\int_{-\infty}^t \int_{-\infty}^{t'} H_2(t - t', t' - t'') u(t') u(t'') dt' dt'' + \dots$$

**Awkward nonlinear**

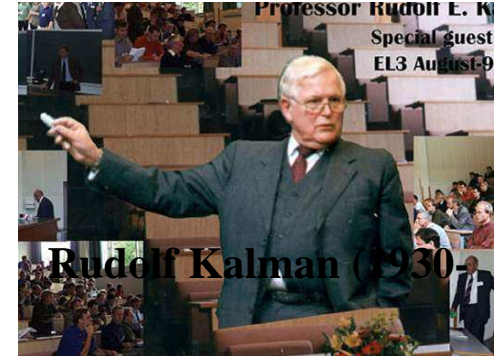
**Far from the physics**

**Fail to deal with 'initial conditions'.**

# Input/state/output systems

Around 1960: a **paradigm shift** to

$$\frac{d}{dt}\mathbf{x} = f(\mathbf{x}, u), \quad \mathbf{y} = g(\mathbf{x}, u)$$



Rudolf Kalman (1930– )

# Input/state/output systems

Around 1960: a **paradigm shift** to

$$\frac{d}{dt}\mathbf{x} = f(\mathbf{x}, u), \quad \mathbf{y} = g(\mathbf{x}, u)$$

1. **open**

**ready to be interconnected**

**outputs of one system  $\mapsto$  inputs of another**

2. **deals with initial conditions**

3. **incorporates nonlinearities, time-variation**

4. **models many physical phenomena**

5. **...**

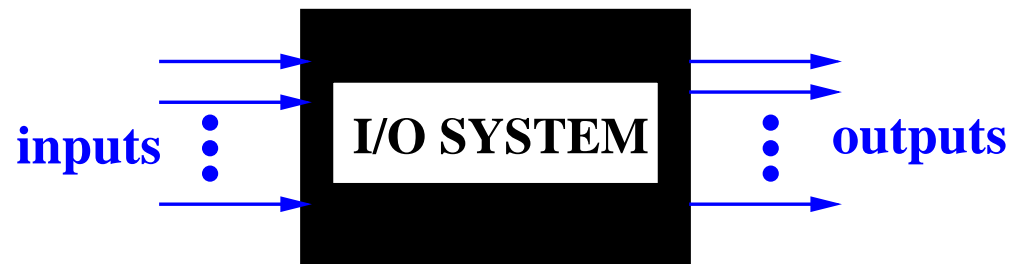
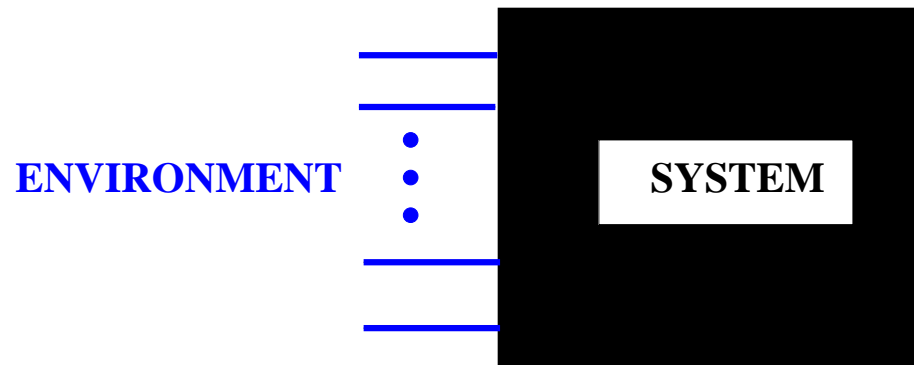




**Theme**

## Theme of this lecture

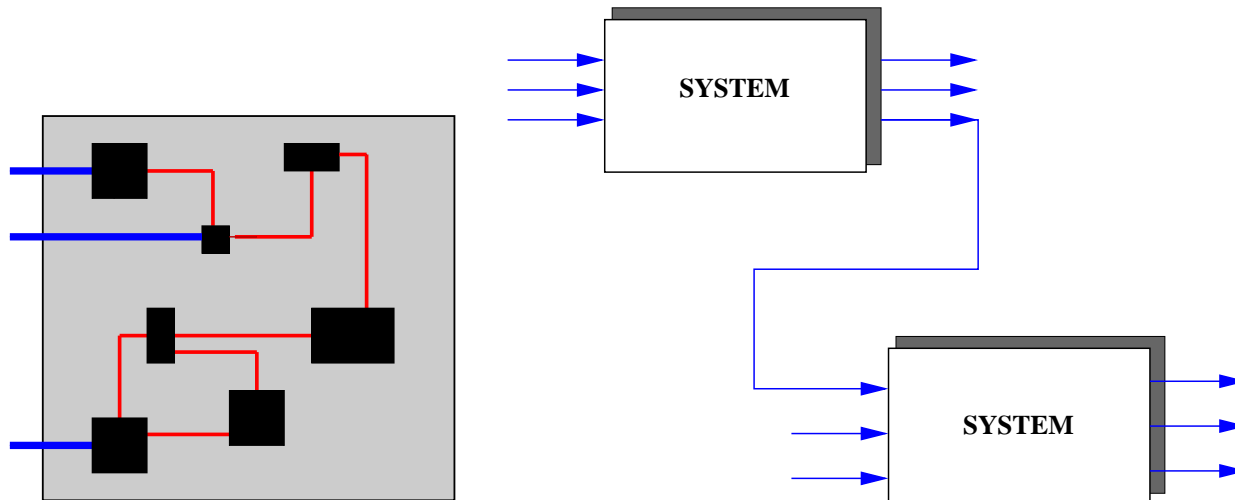
We are accustomed to view an open dynamical system as an **input/output structure**



Is this appropriate for modeling **physical** systems?

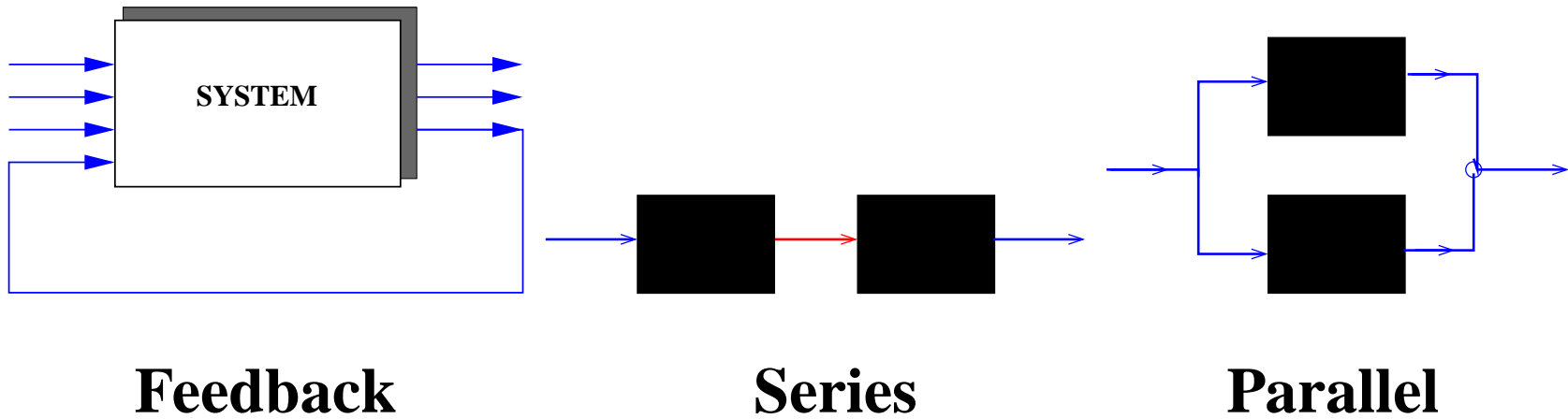
## Theme of this lecture

& interconnection as **output-to-input assignment**.



Is this appropriate for modeling **physical** systems?

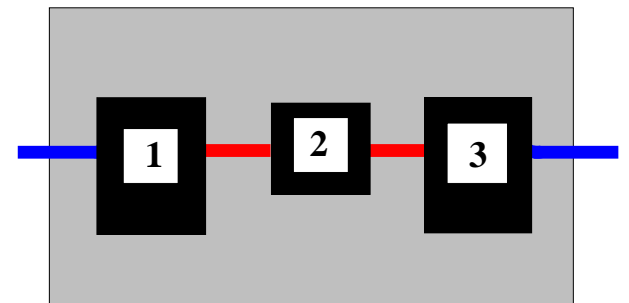
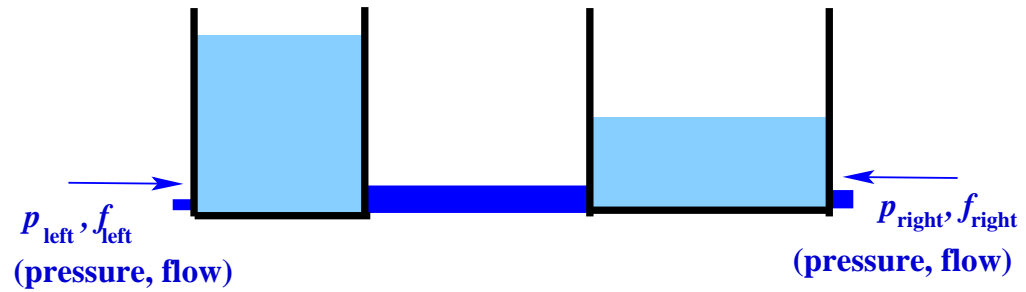
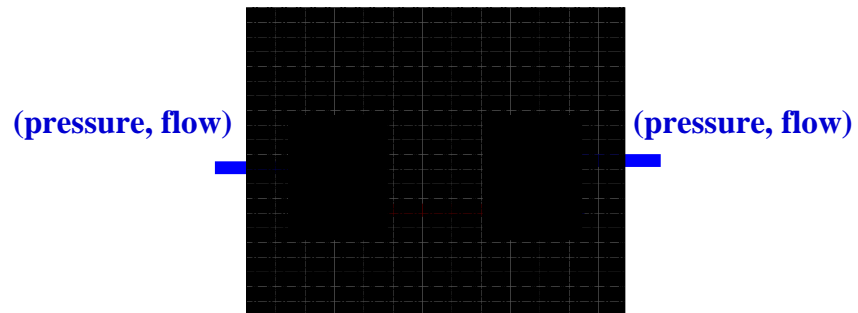
## Theme of this lecture



Is this appropriate for modeling **physical** systems?

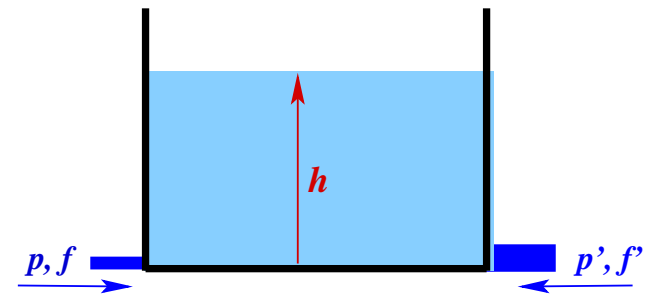
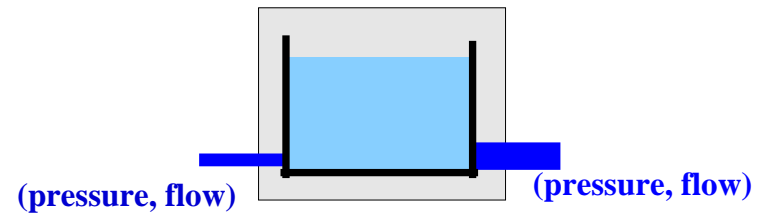
# **Interconnection in physical systems**

# Example



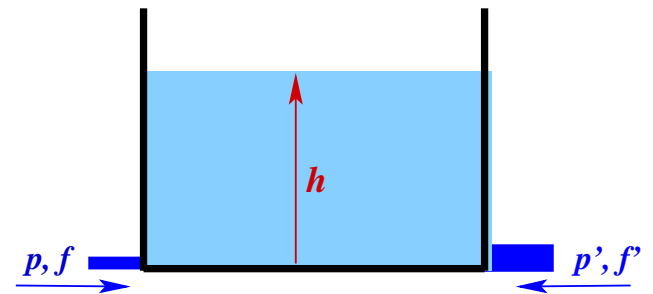
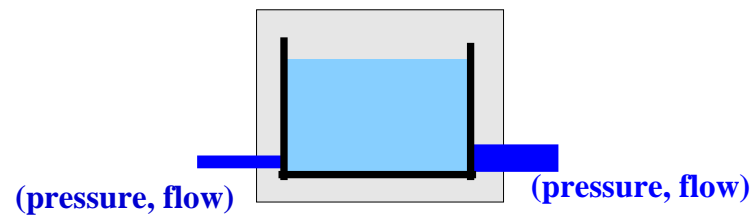
# Example

## Subsystems 1 and 3:



# Example

## Subsystems 1 and 3:



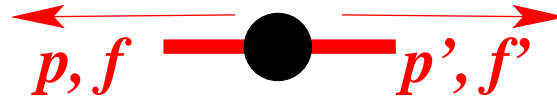
## Subsystem 2:





## Example

Interconnection laws:



$$p = p', \quad f + f' = 0.$$

$$\begin{aligned}
A_1 \frac{d}{dt} h_1 &= f_1 + f'_1, \\
B_1 f_1 &= \begin{cases} \sqrt{|p_1 - p_0 - \rho h_1|} & \text{if } p_1 - p_0 \geq \rho h_1, \\ -\sqrt{|p_1 - p_0 - \rho h_1|} & \text{if } p_1 - p_0 \leq \rho h_1, \end{cases} \\
C f'_1 &= \begin{cases} \sqrt{|p'_1 - p_0 - \rho h_1|} & \text{if } p'_1 - p_0 \geq \rho h_1, \\ -\sqrt{|p'_1 - p_0 - \rho h_1|} & \text{if } p'_1 - p_0 \leq \rho h_1, \end{cases}
\end{aligned} \tag{1}$$

$$f_2 = -f'_2, \quad p_2 - p'_2 = \alpha f_2, \tag{2}$$

$$\begin{aligned}
A_3 \frac{d}{dt} h_3 &= f_3 + f'_3, \\
C f_3 &= \begin{cases} \sqrt{|p_3 - p_0 - \rho h_3|} & \text{if } p_3 - p_0 \geq \rho h_3, \\ -\sqrt{|p_3 - p_0 - \rho h_3|} & \text{if } p_3 - p_0 \leq \rho h_3, \end{cases} \\
C_3 f'_3 &= \begin{cases} \sqrt{|p'_3 - p_0 - \rho h_3|} & \text{if } p'_3 - p_0 \geq \rho h_3, \\ -\sqrt{|p'_3 - p_0 - \rho h_3|} & \text{if } p'_3 - p_0 \leq \rho h_3, \end{cases}
\end{aligned} \tag{3}$$

$$p'_1 = p_2, \quad f'_1 + f_2 = 0, \quad p'_2 = p_3, \quad f'_2 + f_3 = 0. \tag{4}$$

$$p_{\text{left}} = p_1, \quad f_{\text{left}} = f_1, \quad p_{\text{right}} = p'_3, \quad f_{\text{right}} = f'_3. \tag{5}$$

- **Unclear input/output structure for terminal variables**
- **Many variables, indivisibly, at the same terminal**
- **Interconnection = variable sharing**
- **No signal flows, no output-to-input assignment**

- Unclear input/output structure for terminal variables
- Many variables, indivisibly, at the same terminal
- Interconnection = variable sharing
- No signal flows, no output-to-input assignment

*“Block diagrams unsuitable for serious physical modeling*

*- the control/physics barrier”*

*“Behavior based (declarative) modeling is a good alternative”*



from K.J. Åström, *Present Developments in Control Applications*



**IFAC 50-th Anniversary Celebration  
Heidelberg, September 12, 2006.**

# **Behavioral systems**

**A dynamical system**

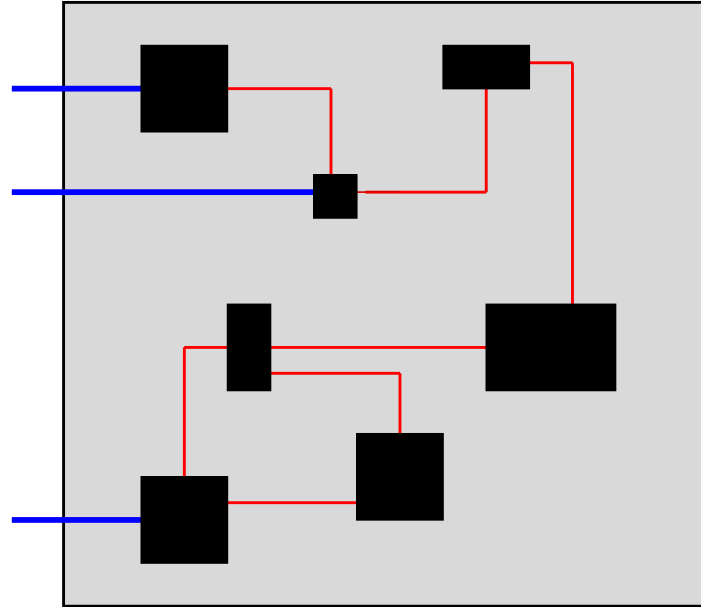
:  $\Leftrightarrow$  a family of time functions, *'the behavior'*

**Interconnection** :  $\Leftrightarrow$  *'variable sharing'*.

**Control** :  $\Leftrightarrow$  *interconnection*.

**Modeling of interconnected physical systems is the strongest case for 'behaviors'.**

# Objective



To develop a mathematical framework for dealing with interconnection of (**open**, dynamical) systems.

## Objective

To develop a mathematical framework for dealing with interconnection of (**open**, dynamical) systems.

### Competing philosophies:

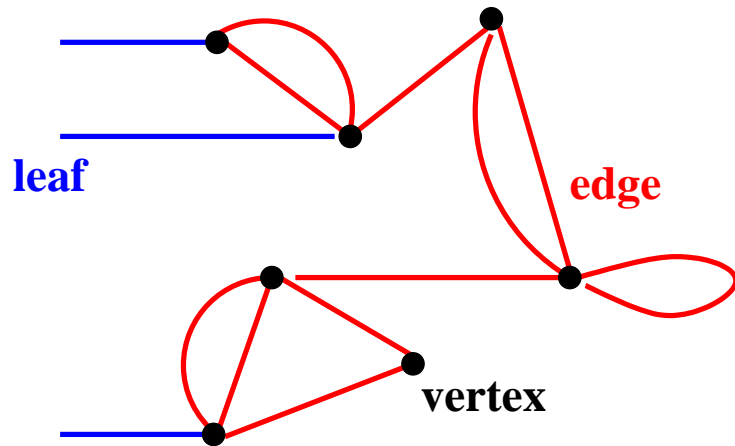
- input/output signal flow graphs
- circuit diagrams (loops, nodes)
- bond graphs (across, through, power)
- object-oriented modeling (SPICE, Modelica, ...)
- ...



# Formalization of interconnection architecture

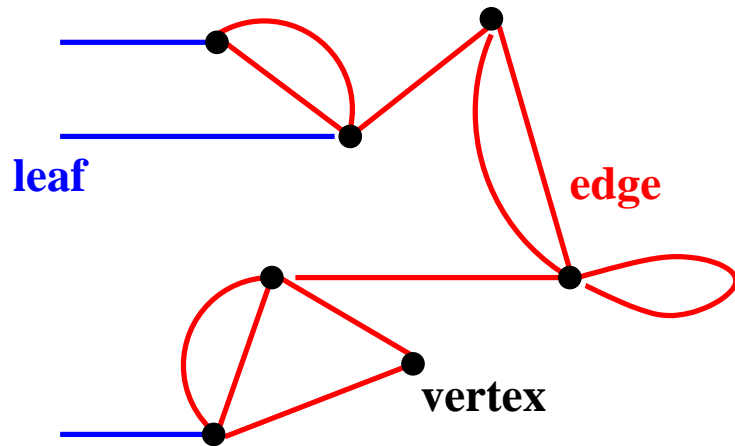
# Architecture & module embedding

## Architecture

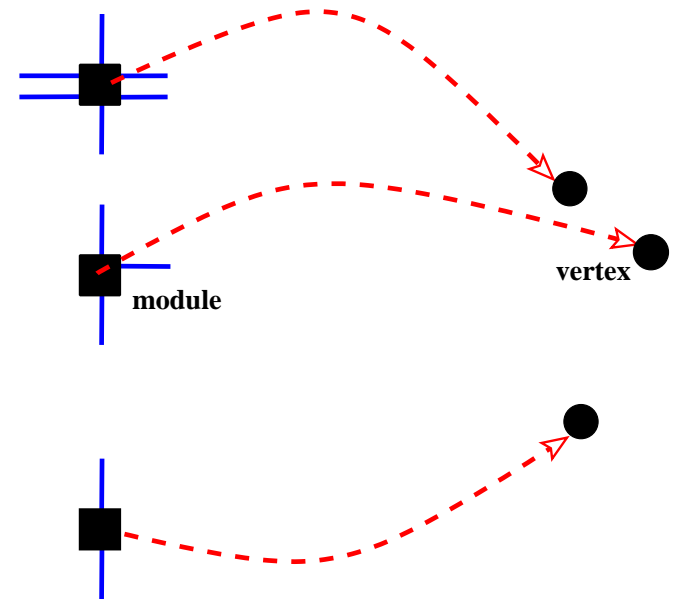


# Architecture & module embedding

## Architecture

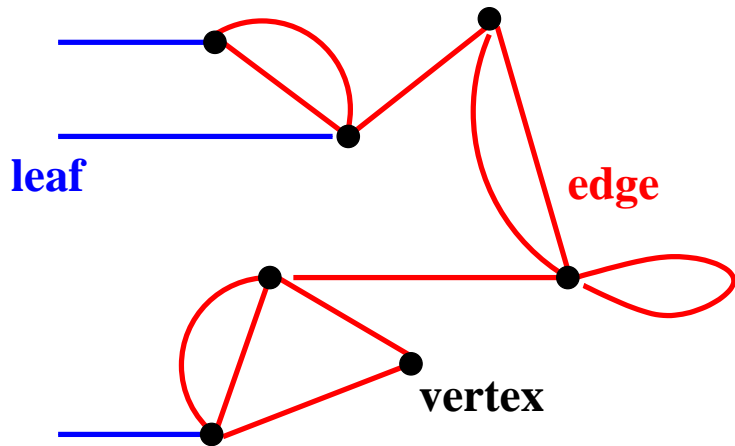


## Modules (systems) in the vertices

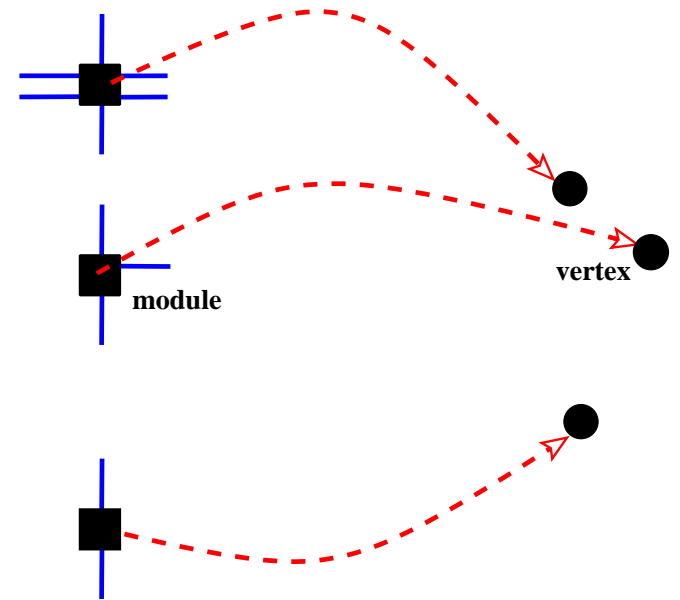


# Architecture & module embedding

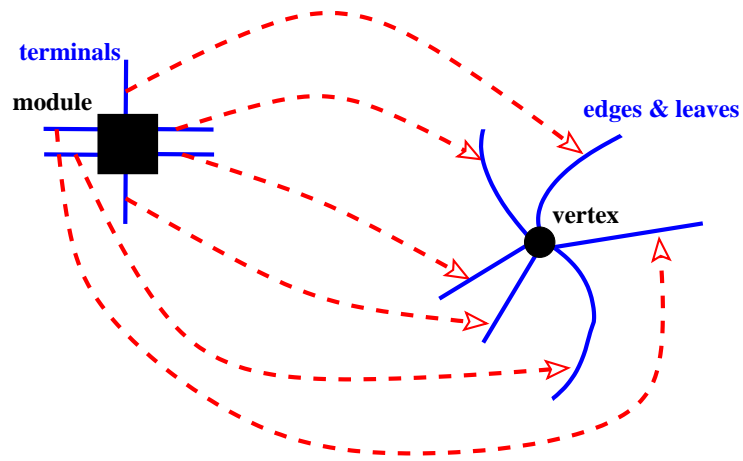
## Architecture



## Modules (systems) in the vertices



## Terminals in the edges



## Interconnection architecture

A **graph with leaves** defined as  $\mathcal{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, \mathcal{A})$

$\mathbb{V}$  the set of *vertices*,

$\mathbb{E}$  the set of *edges*,

$\mathbb{L}$  the set of *leaves*,

$\mathcal{A}$  the *adjacency map*.

$\mathcal{A}$  associates

with each edge  $e \in \mathbb{E}$  an unordered pair

$$\mathcal{A}(e) = [v_1, v_2] \quad v_1, v_2 \in \mathbb{V},$$

with each leaf  $\ell \in \mathbb{L}$  an element  $\mathcal{A}(\ell) = v \in \mathbb{V}$ .

## Module embedding

The *module embedding* associates  
a module with each vertex,  
a  $1 \leftrightarrow 1$  assignment between the  
edges and leaves adjacent to the vertex and  
the terminals of the module.

## Module embedding

The **module embedding** associates  
a module with each vertex,  
a  $1 \leftrightarrow 1$  assignment between the  
edges and leaves adjacent to the vertex and  
the terminals of the module.

**Vertices** specify the subsystems,  
**edges** how terminals of subsystems are connected,  
**leaves** how the interconnected system interacts with the  
environment.

# Module embedding

**Vertices**  $\rightsquigarrow$  **Subsystems**

**Edges**  $\rightsquigarrow$  **Interconnections**



## Manifest variables

The *manifest variable assignment* is a map that assigns the manifest variables as a function of the terminal (or, more general, the module) variables.

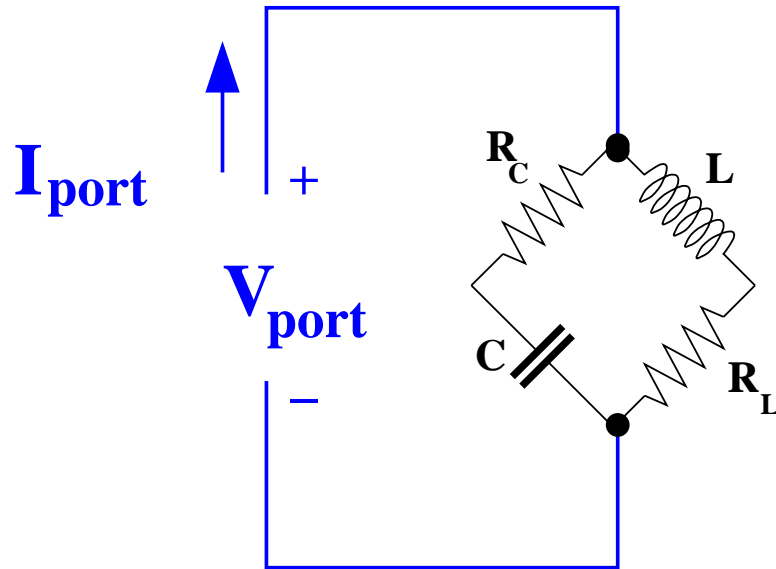
The terminal variables are henceforth considered as latent variables.

## Behavioral equations

1. **Module equations** for each vertex.  
Relation among the variables on the terminals of the subsystems.
2. **Interconnection equations** for each edge.  
Equating the variables on the terminals associated with the same edge.
3. **Manifest variable assignment**  
Specifies the variables of interest.

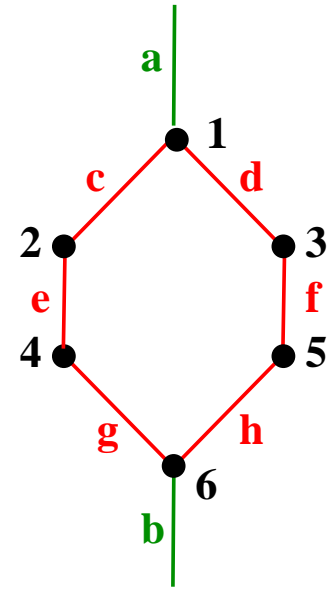
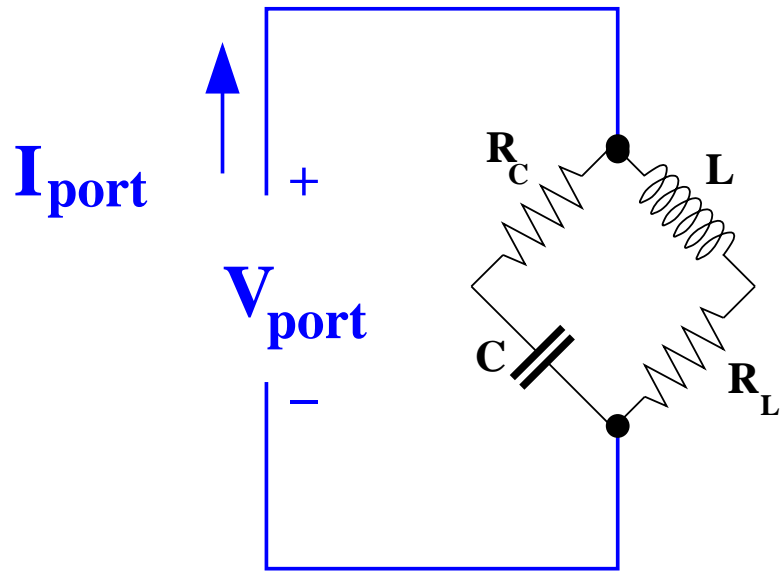
**A very classical example**

# RLC circuit

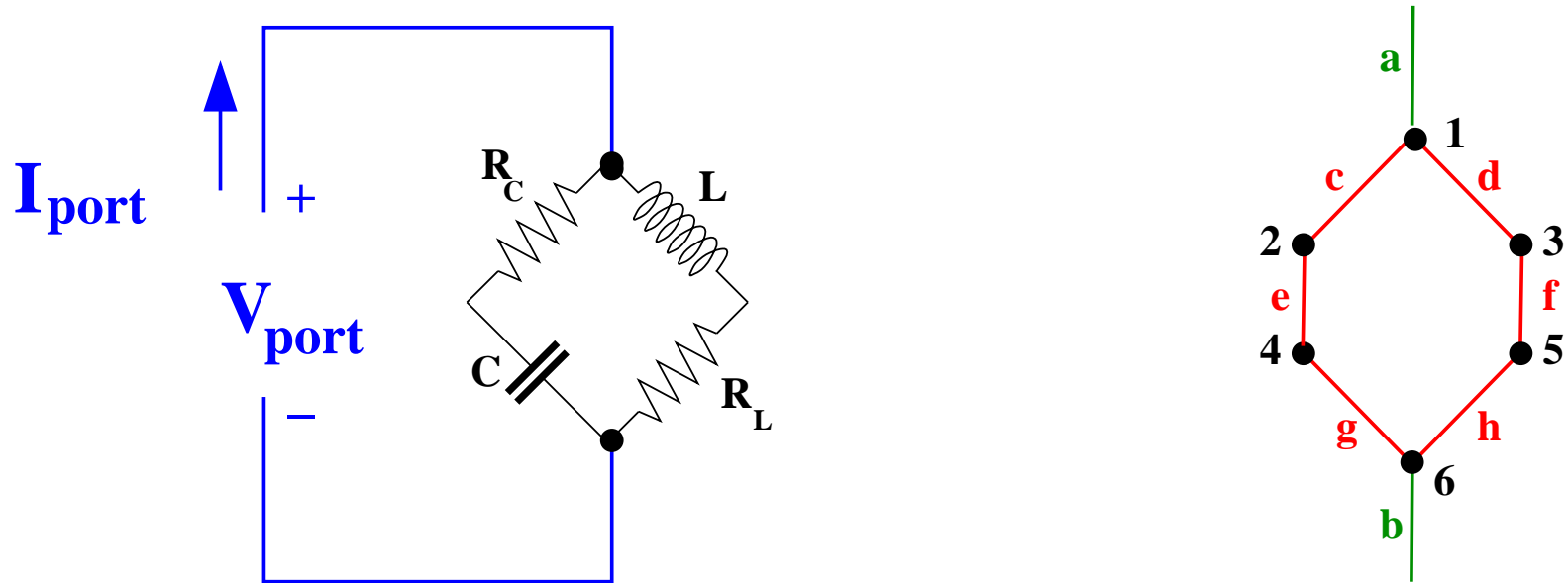


!!! Model the port behavior !!!

# RLC circuit



# RLC circuit



$$R_C \mapsto 2, R_L \mapsto 5, C \mapsto 4, L \mapsto 3, \text{connector}_1 \mapsto 1, \text{connector}_2 \mapsto 6,$$

$$1_{R_C} \mapsto c, 2_{R_C} \mapsto e, 1_{R_L} \mapsto f, 2_{R_L} \mapsto h, 1_C \mapsto e, 2_C \mapsto g, 1_L \mapsto d, 2_L \mapsto f,$$

$$1_{\text{connector}_1} \mapsto a, 2_{\text{connector}_1} \mapsto c, 3_{\text{connector}_1} \mapsto d,$$

$$1_{\text{connector}_2} \mapsto b, 2_{\text{connector}_2} \mapsto g, 3_{\text{connector}_2} \mapsto h.$$

## Module equations

**vertex 1**

$$V_{1_{\text{connector}_1}} = V_{2_{\text{connector}_1}} = V_{3_{\text{connector}_1}},$$
$$I_{1_{\text{connector}_1}} + I_{2_{\text{connector}_1}} + I_{3_{\text{connector}_1}} = 0;$$

**vertex 2**

$$V_{1_{R_C}} - V_{2_{R_C}} = R_C I_{1_{R_C}}, \quad I_{1_{R_C}} + I_{2_{R_C}} = 0;$$

**vertex 3**

$$L \frac{d}{dt} I_{I_L} = V_{1_L} - V_{2_L}, \quad I_{1_L} + I_{2_L} = 0;$$

**vertex 4**

$$C \frac{d}{dt} (V_{1_C} - V_{2_C}) = I_{1_C}, \quad I_{1_C} + I_{2_C} = 0;$$

**vertex 5**

$$V_{1_{R_L}} - V_{2_{R_L}} = R_L I_{1_{R_L}}, \quad I_{1_{R_L}} + I_{2_{R_L}} = 0;$$

**vertex 6**

$$V_{1_{\text{connector}_2}} = V_{2_{\text{connector}_2}} = V_{3_{\text{connector}_2}},$$
$$I_{1_{\text{connector}_2}} + I_{2_{\text{connector}_2}} + I_{3_{\text{connector}_2}} = 0.$$

## Interconnection equations

**edge c**

$$V_{1_{RC}} = V_{2_{\text{connector}_1}}, I_{1_{RC}} + I_{2_{\text{connector}_1}} = 0;$$

**edge d**

$$V_{1_L} = V_{3_{\text{connector}_1}}, I_{1_L} + I_{3_{\text{connector}_1}} = 0;$$

**edge e**

$$V_{2_{RC}} = V_{1_C}, I_{2_{RC}} + I_{1_C} = 0;$$

**edge f**

$$V_{2_L} = V_{1_{RC}}, I_{2_L} + I_{1_{RC}} = 0;$$

**edge g**

$$V_{2_C} = V_{1_{\text{connector}_2}}, I_{2_C} + I_{1_{\text{connector}_2}} = 0;$$

**edge h**

$$V_{2_{RL}} = V_{2_{\text{connector}_2}}, I_{2_{RL}} + I_{2_{\text{connector}_2}} = 0.$$



## Manifest variable assignment

$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

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$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

**The module equations**

**+ the interconnection constraints**

**+ the manifest variable assignment**

**form the complete model for the behavior of**

$$(V_{\text{external port}}, I_{\text{external port}})$$

**Prevalence of latent variables  $\rightsquigarrow$  elimination theory.**

## Manifest variable assignment

$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

**Behavior = all**

$$(V_{\text{external port}}, I_{\text{external port}}) : \mathbb{R} \rightarrow \mathbb{R}^2$$

$\exists \dots, V_{1_{R_c}}, \dots, I_{3_{\text{connector}_2}} \mathbb{R} \rightarrow \mathbb{R}^{\dots}$  **such that ...**

## Manifest behavior

$\rightsquigarrow$  the dynamical system  $\Sigma = (\mathbb{R}, \mathbb{R}^2, \mathcal{B})$  with behavior  $\mathcal{B}$  specified by:

Case 1:  $CR_C \neq \frac{L}{R_L}$

$$\left( \frac{R_C}{R_L} + \left( 1 + \frac{R_C}{R_L} \right) CR_C \frac{d}{dt} + CR_C \frac{L}{R_L} \frac{d^2}{dt^2} \right) \mathbf{V} = \left( 1 + CR_C \frac{d}{dt} \right) \left( 1 + \frac{L}{R_L} \frac{d}{dt} \right) R_C \mathbf{I}$$

Case 2:  $CR_C = \frac{L}{R_L}$

$$\left( \frac{R_C}{R_L} + CR_C \frac{d}{dt} \right) \mathbf{V} = (1 + CR_C) \frac{d}{dt} R_C \mathbf{I}$$

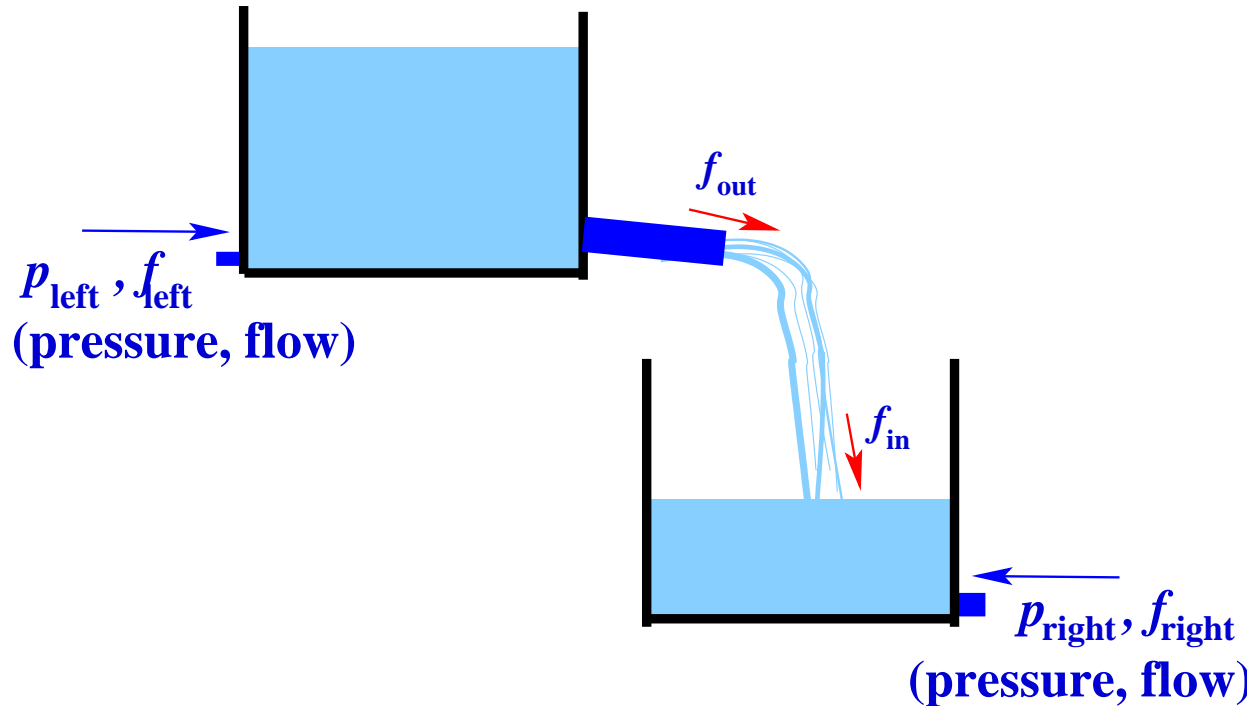
$\rightsquigarrow$  behavior  $\mathcal{B} =$  all solutions  $(V, I) : \mathbb{R} \rightarrow \mathbb{R}^2$

# Other methodologies

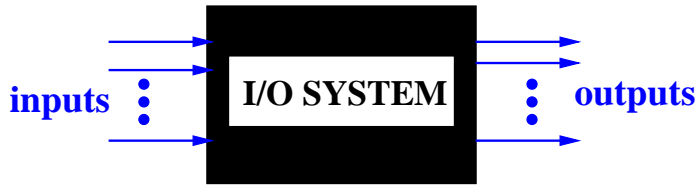
# Signal flow graphs

## input/output thinking

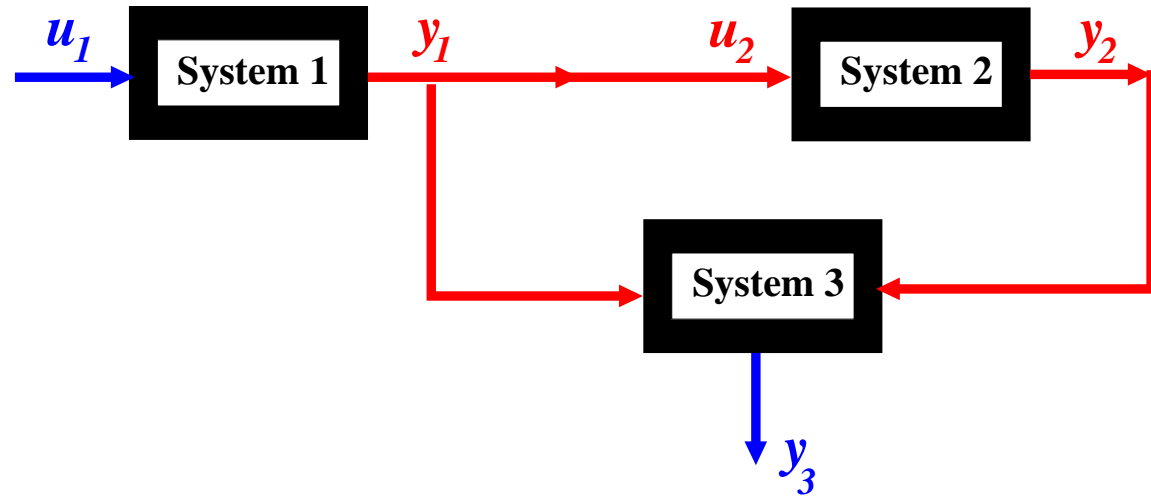
There are many many examples where output-to-input connection is eminently natural:



# input/output thinking



(a)

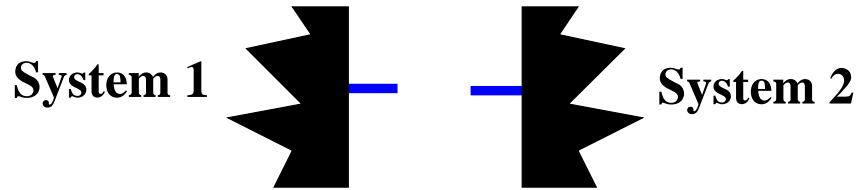


(b)

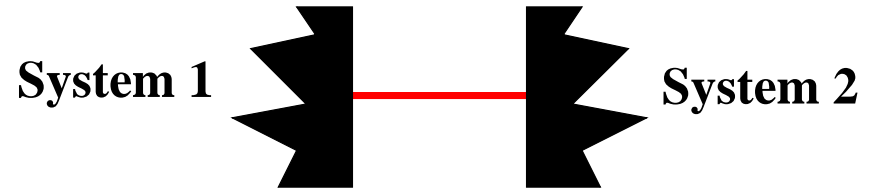
- shows terminal variables separate
- suggests that inputs and outputs occur at different points
- allows impossible input-output connections



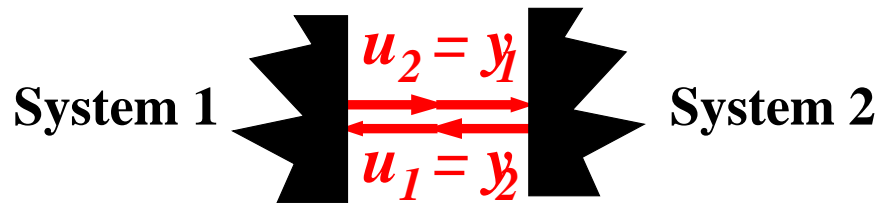
# input/output thinking



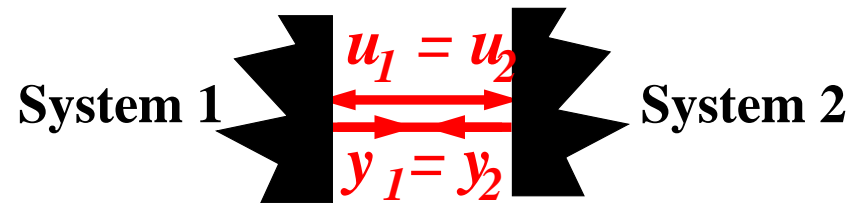
(a)



(b)



(c)



(d)

For physical systems

**input-to-input** & **output-to-output**

assignment very prevalent.

Physical systems are not signal processors.

# Bond graphs

# Bond graphs

Interconnection variables:

a **flow** and an **effort**

**product = power**

- **current & voltage**
- **velocity & force**
- **mass flow & pressure**
- **heat flow & temperature**  
 $\frac{\text{heat flow}}{\text{temperature}}$  & temperature
- ...

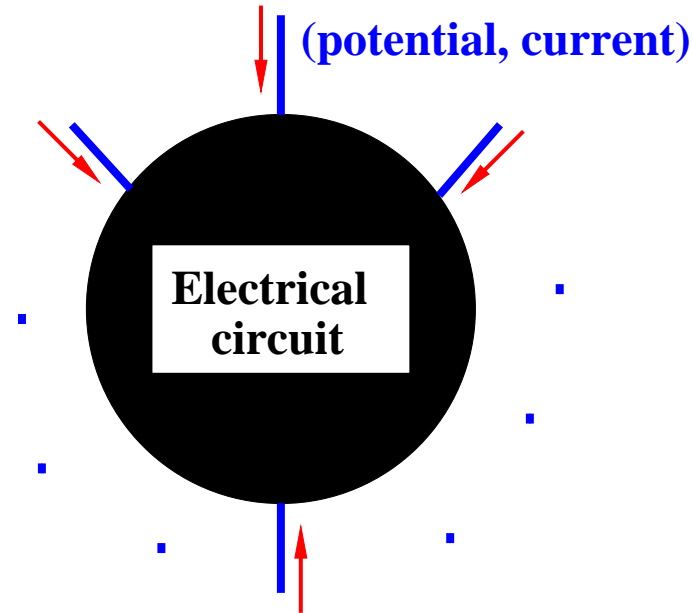
## Bond graphs

**Interconnection variables:**

a **flow** and an **effort** **product = power**

- 1. Mechanical interconnections equate positions, not velocities**
- 2. Not all interconnections involve equating energy transfer**
- 3. Terminals are for interconnection, ports are for energy transfer**

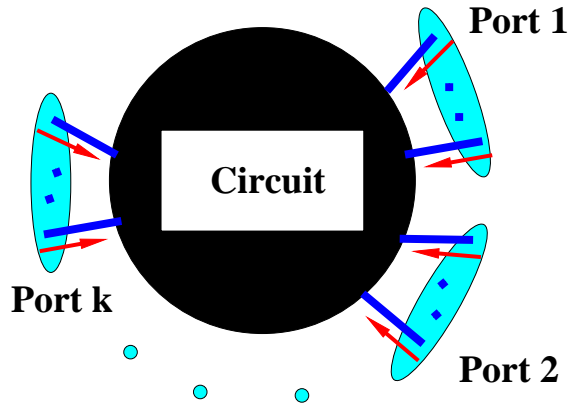
# Terminals versus ports



**Terminal variables and behavior:**

$$(V_1, I_1, V_2, I_2, \dots, V_n, I_n) \rightsquigarrow \text{behavior } \mathcal{B} \subseteq \left( \mathbb{R}^{2n} \right)^{\mathbb{R}}$$

# Terminals versus ports



**Port**  $:\Leftrightarrow$  **sum currents = 0**  
**potentials + constant  $\Rightarrow$  potentials**

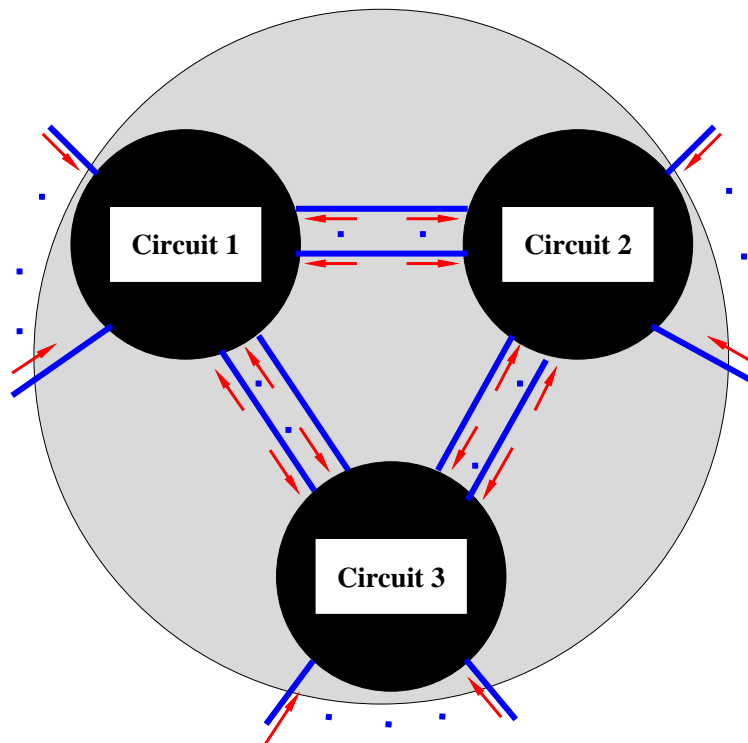
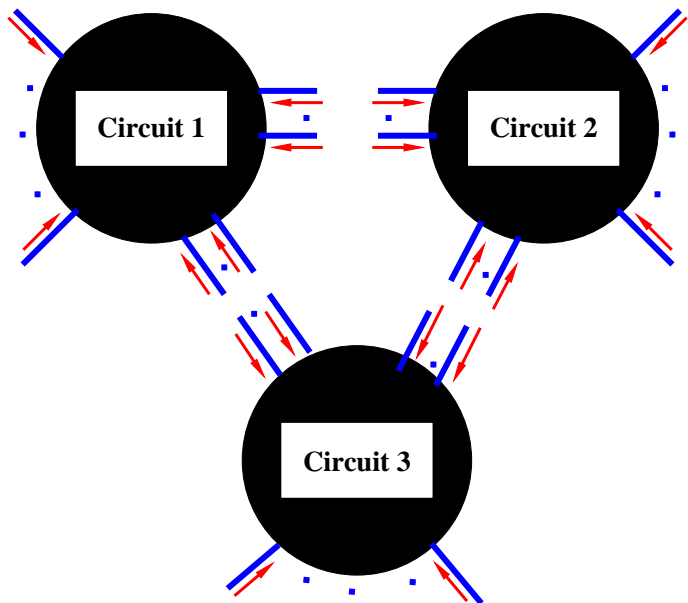
$$\left( \boxed{V_1, I_1, \dots, V_p, I_p}, V_{p+1}, \dots, I_n \right) \in \mathcal{B}, \alpha : \mathbb{R} \rightarrow \mathbb{R}$$



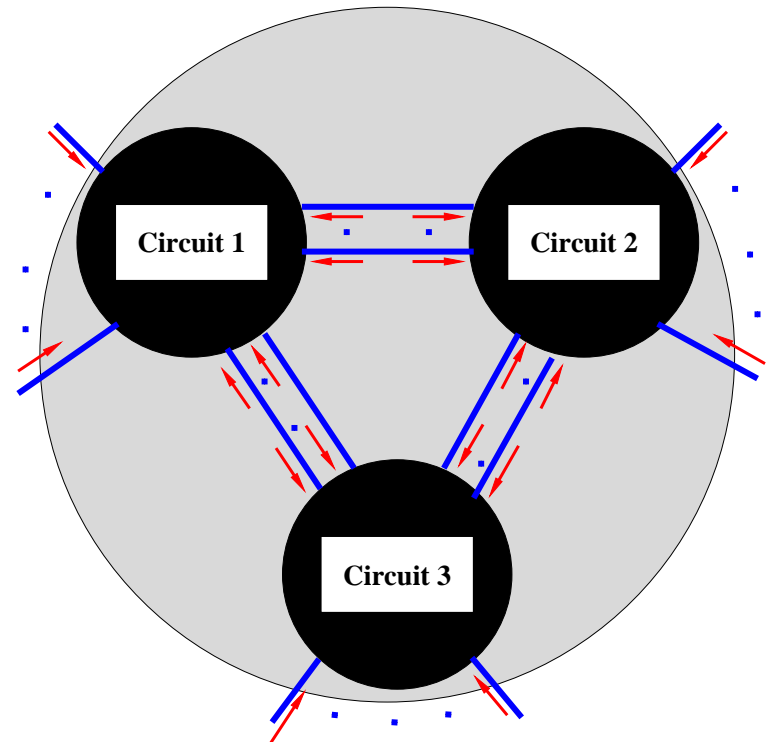
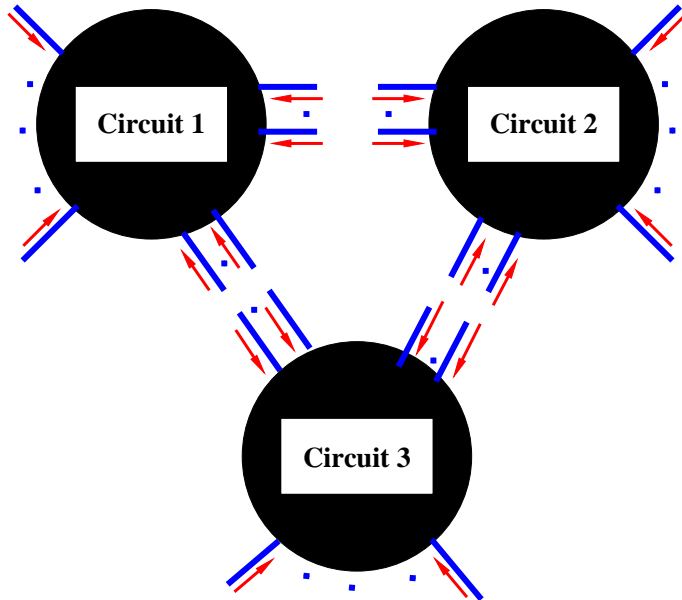
$$\left( \boxed{V_1 + \alpha, I_1, \dots, V_p + \alpha, I_p}, V_{p+1}, \dots, I_n \right) \in \mathcal{B}$$

$$\boxed{I_1 + \dots + I_p} = 0$$

# Terminals versus ports



## Terminals versus ports



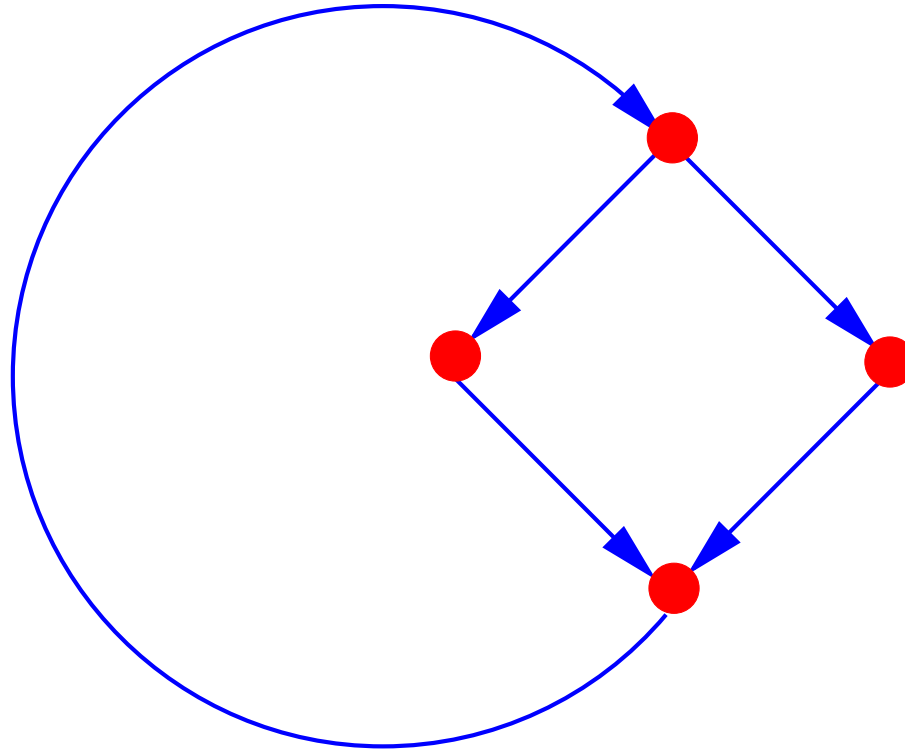
**Interconnection via terminals, energy transfer via ports; one cannot talk about**

***“the energy transferred from circuit 1 to circuit 2”***



# Circuit diagrams

## Circuit diagrams



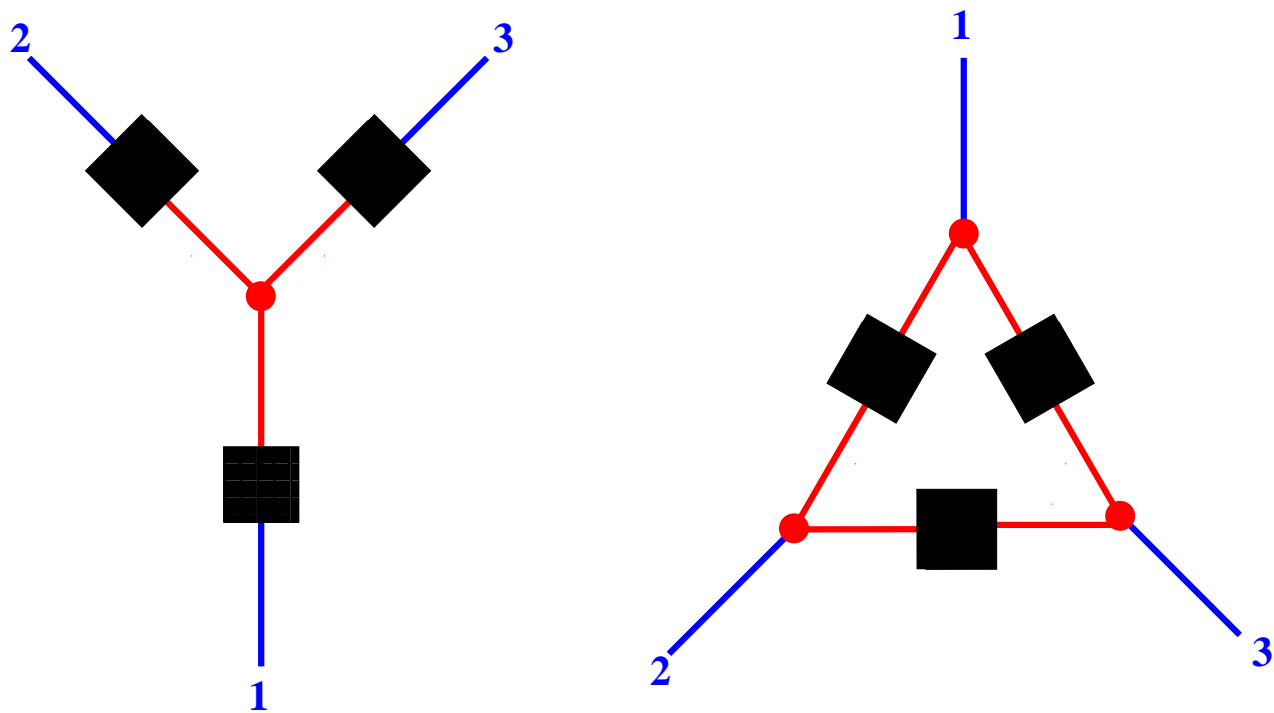
**Circuit diagrams with**

**nodes & branches & KVL & KCL**

**are only effective with 2-terminal 1-ports.**

# Circuit diagrams

**Not closed under composition**



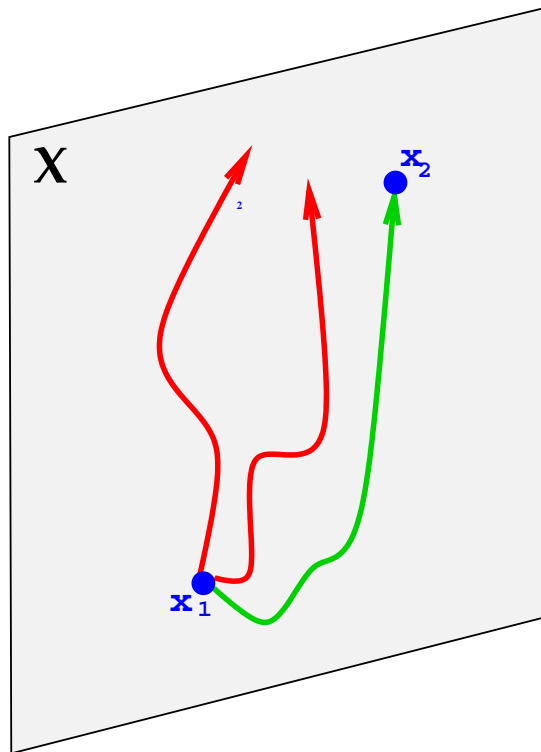
# Various facets of control

## Path planning

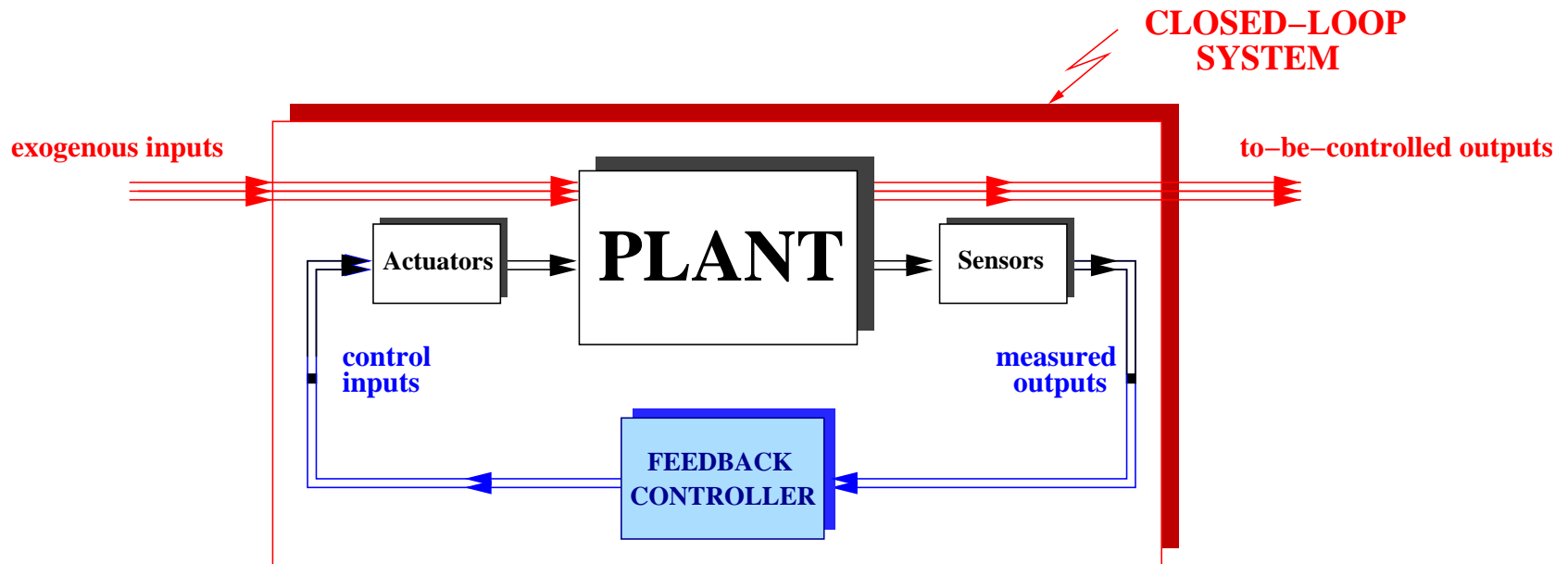
$$\frac{d}{dt}x = f(x, u)$$

Choose time-function  $u(\cdot) : [0, T] \rightarrow \mathbb{U}$  so as to achieve (optimal) state transfer.

‘open loop control’



# Decision making



Choose **map from sensor outputs to actuator inputs** so as to achieve good (optimal) performance.

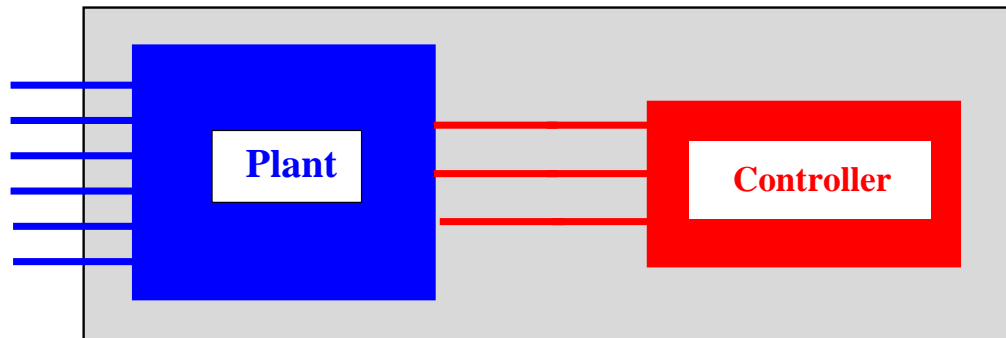
**‘feedback control’**

**‘closed loop control’**

**‘intelligent control’**

# Embedded control

# Embedded systems

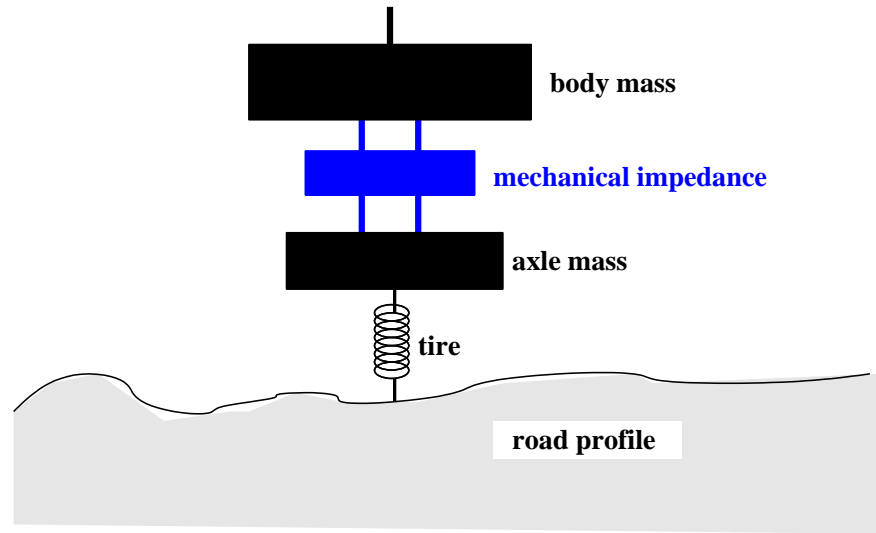
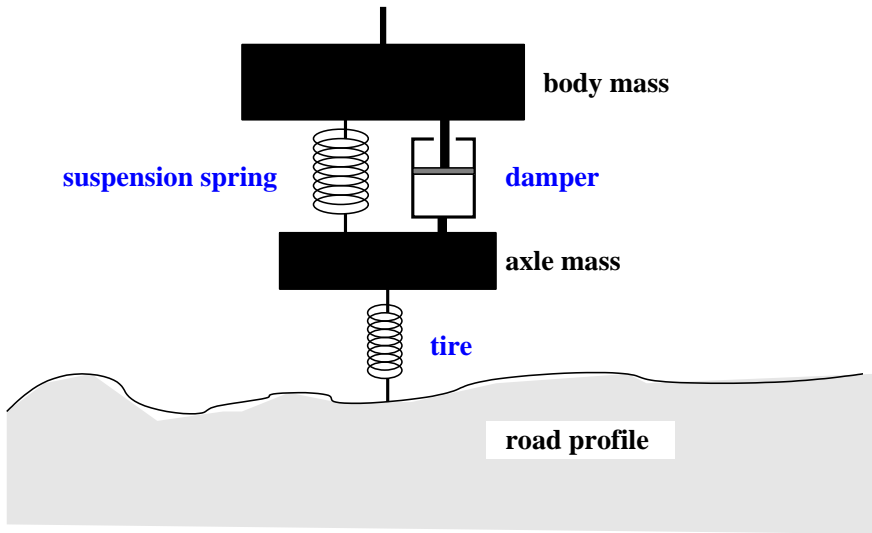


Choose **controller** so as to achieve good (optimal) performance of the interconnected system

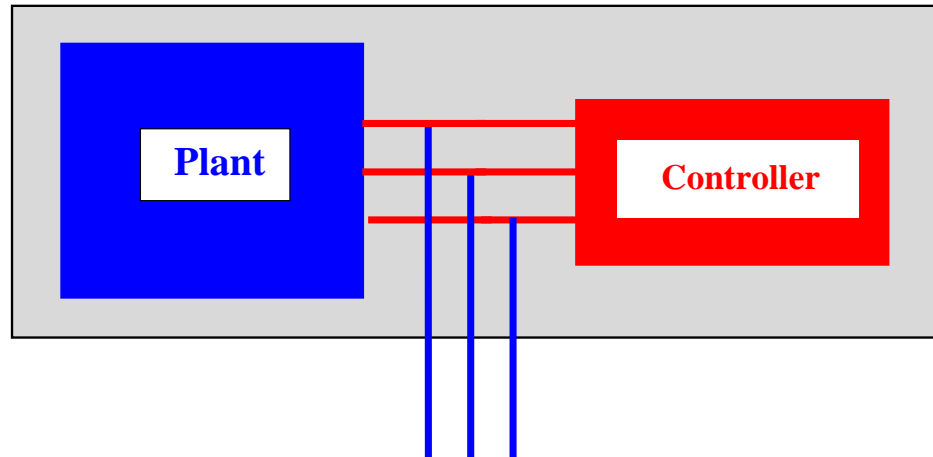
‘control as interconnection’  
‘**integrated system design**’



# Example

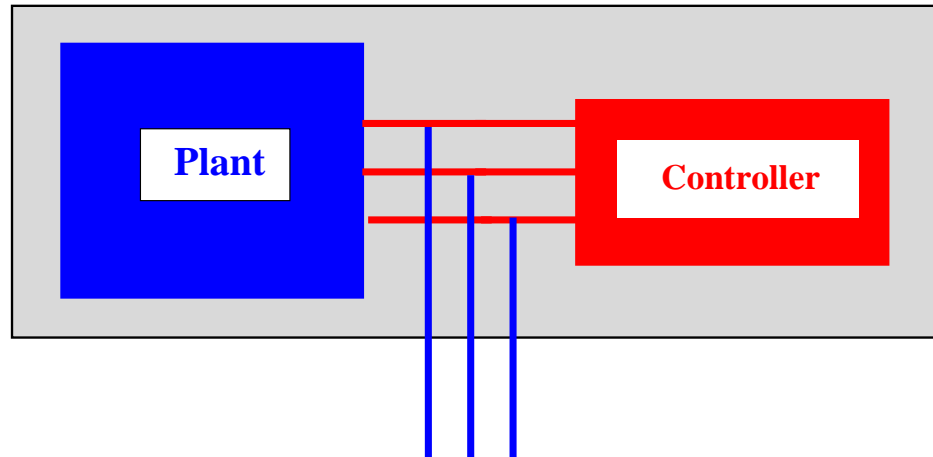


## Control as interconnection



**Plant behavior  $\mathcal{P}$ , controller behavior  $\mathcal{K}$ ,  
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## Robustness

**Robust stability, but**  $\left\| \frac{1}{s} - \frac{1}{s+a} \right\| = \infty$ .

## Robustness

Viewing plant as a behavior, rather than i/o map  $\rightsquigarrow$

**Robustness**: Given  $\mathcal{P}$ , stabilized by  $\mathcal{K}$ , how close to  $\mathcal{P}$  needs  $\mathcal{P}'$  be to be also stabilized by  $\mathcal{K}$ ?

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# Overview



## Conclusions

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- **Views control as interconnection**
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- **Far easier pedagogically**
- **...**

**Details & copies of frames are available from/at**

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<http://www.esat.kuleuven.be/~jwillems>

**Thank you**

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