



SYSTEM INTERCONNECTION

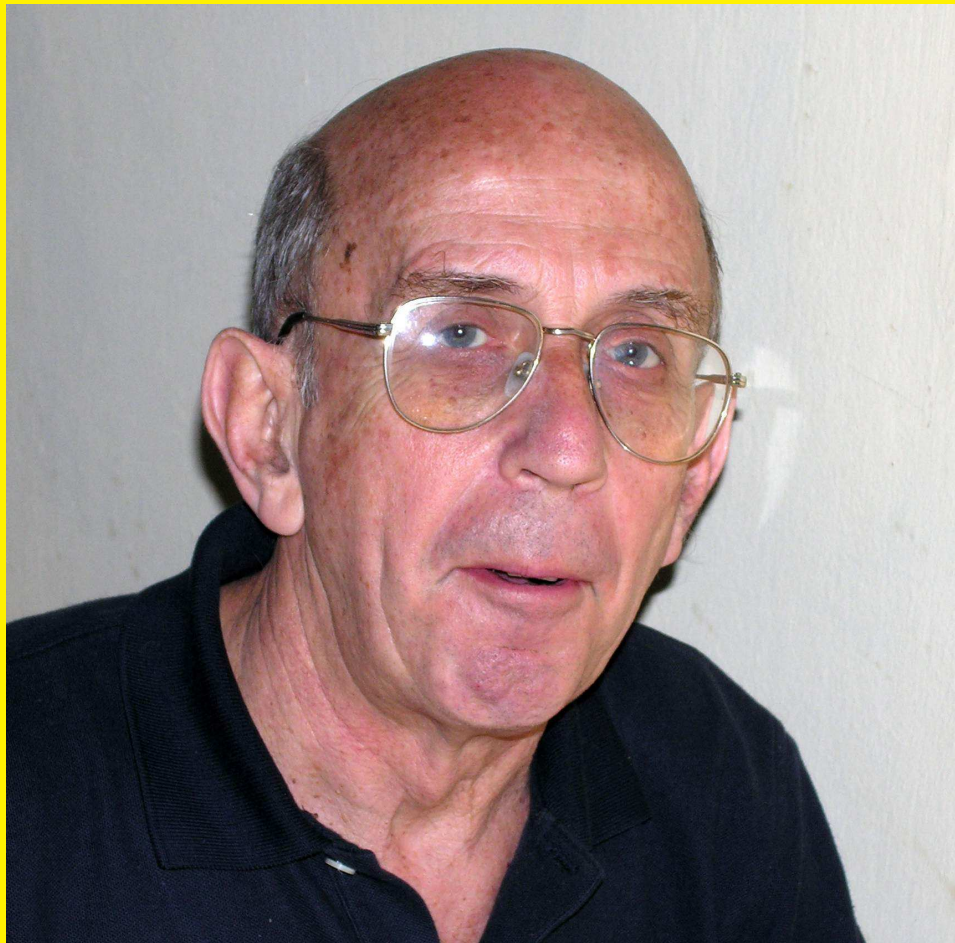
Jan C. Willems

K.U. Leuven, Flanders, Belgium

IsidoriFest

London, May 16, 2008

On the occasion of Alberto's 65-th



Spedizione in abb. postale - Gruppo IV

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SPECIAL ISSUE ON SYSTEM THEORY AND PHYSICS

Edited by R. W. Brockett

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EDITOR

ANTONIO RUBERTI
Istituto di Automatica
Università di Roma
Via Eudossiana, 18
00184 ROMA
ITALY

ASSOCIATE EDITORS

GUIDO GUARDABASSI
Istituto di Elettrotecnica ed Elettronica
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Istituto di Automatica
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Istituto di Automatica
Università di Roma
Via Eudossiana, 18
00184 ROMA
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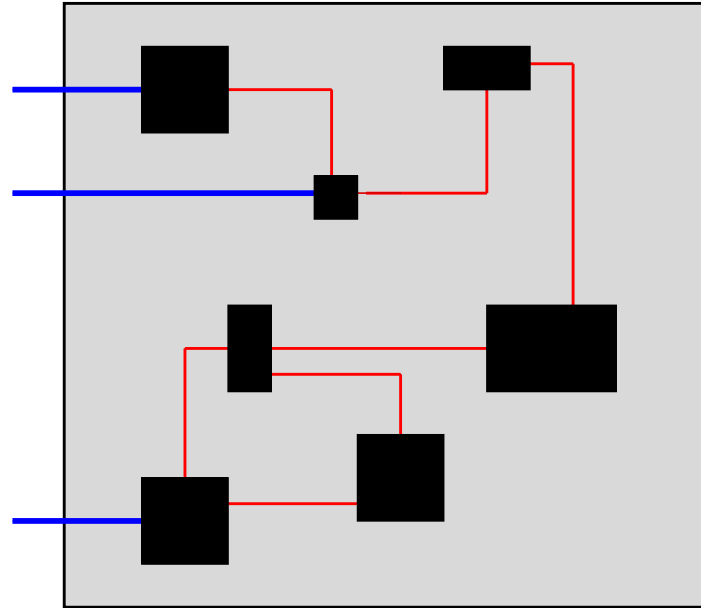
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Objective



To develop a mathematical framework for dealing with interconnection of (open**, dynamical) systems.**

Objective

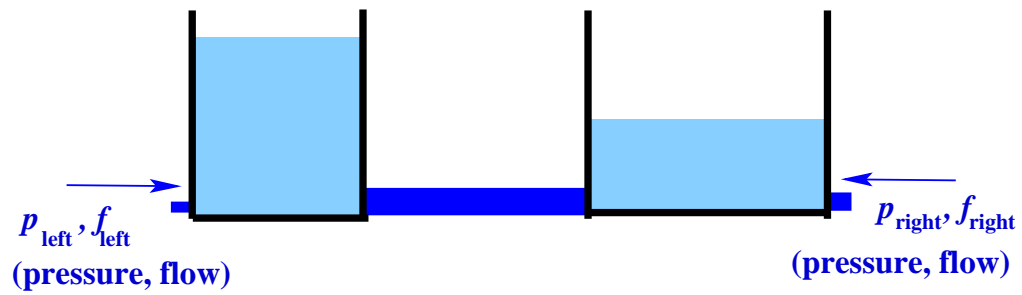
To develop a mathematical framework for dealing with interconnection of (open**, dynamical) systems.**

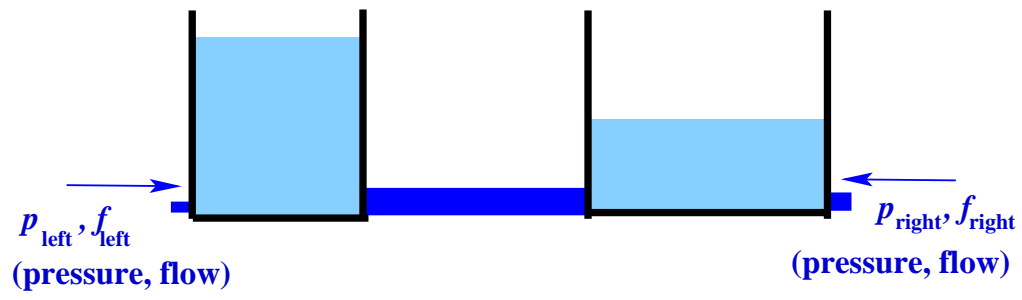
Competing philosophies:

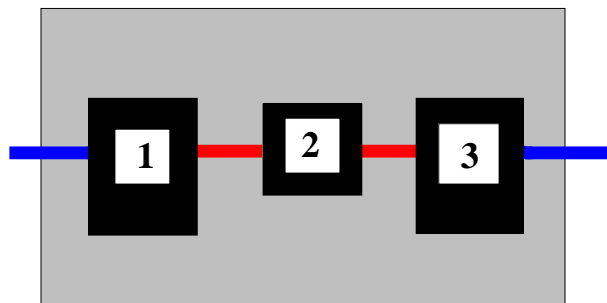
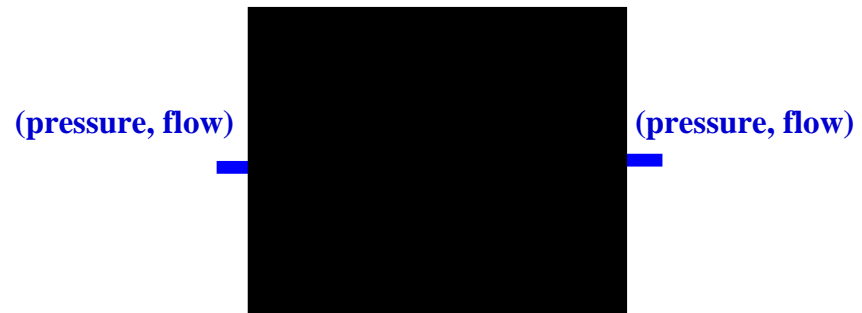
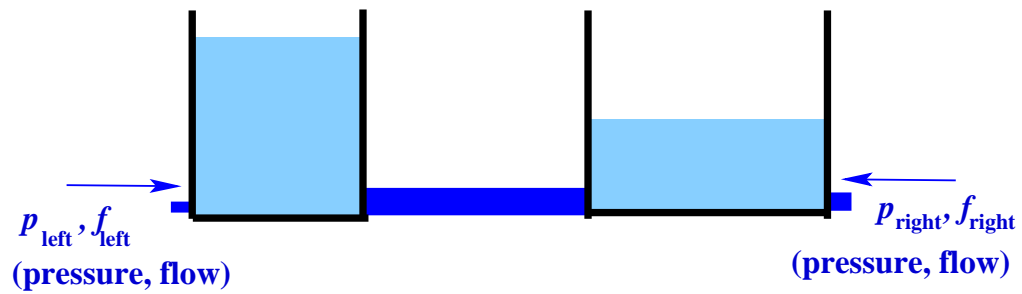
- **input/output signal flow graphs**
- **circuit diagrams (loops, nodes)**
- **bond graphs (across, through, power)**
- **object-oriented modeling (SPICE, Modelica, ...)**
- **...**

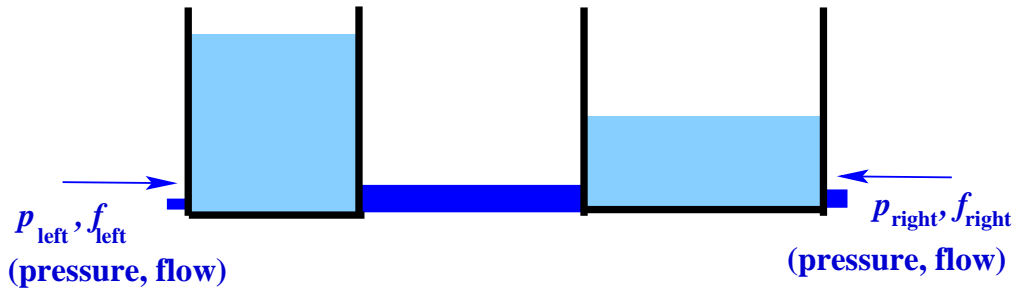
A simple example



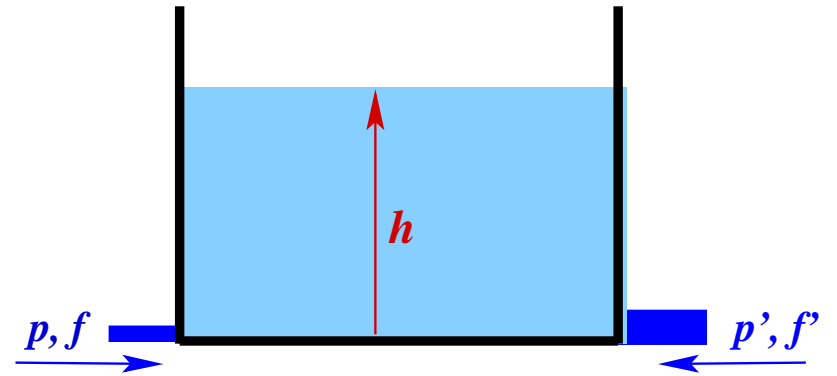
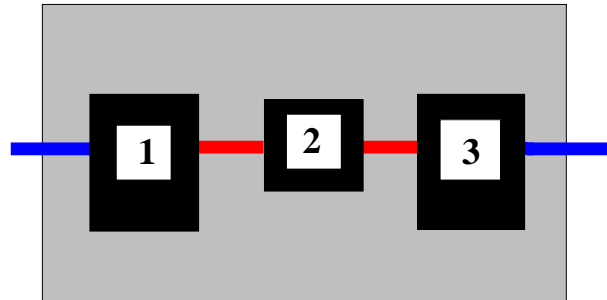


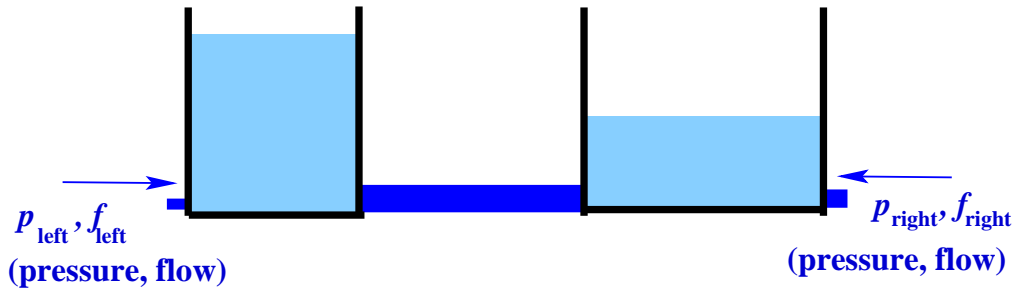




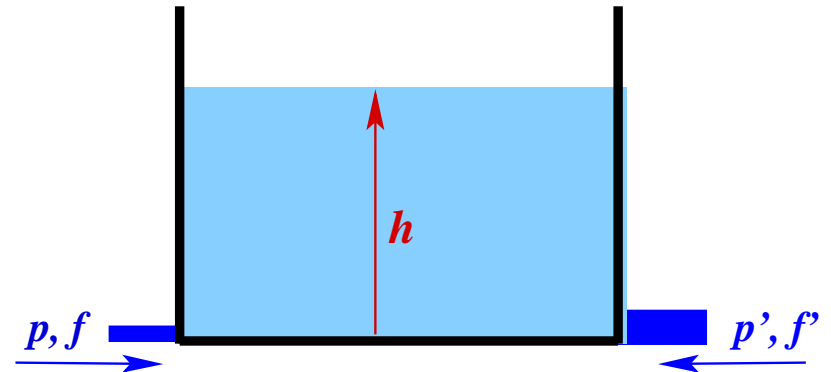
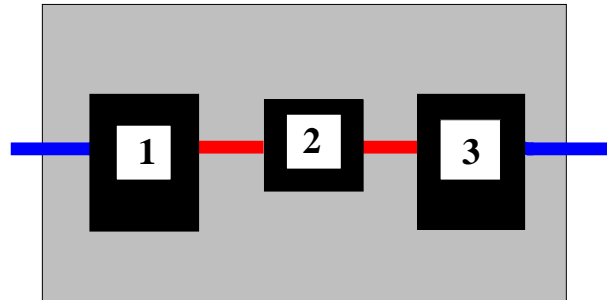


black box 1 & 3



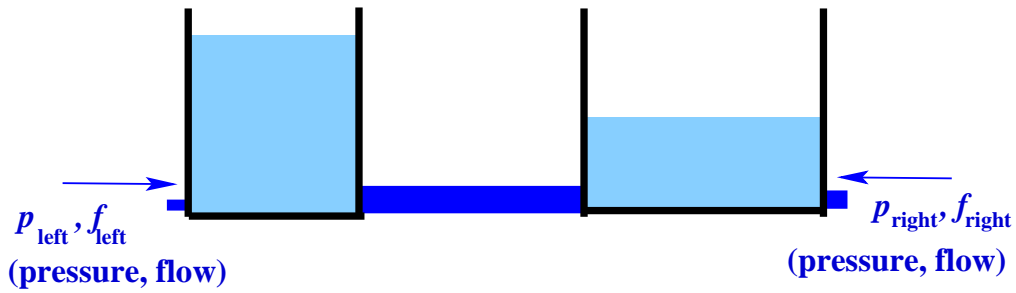


black box 1 & 3

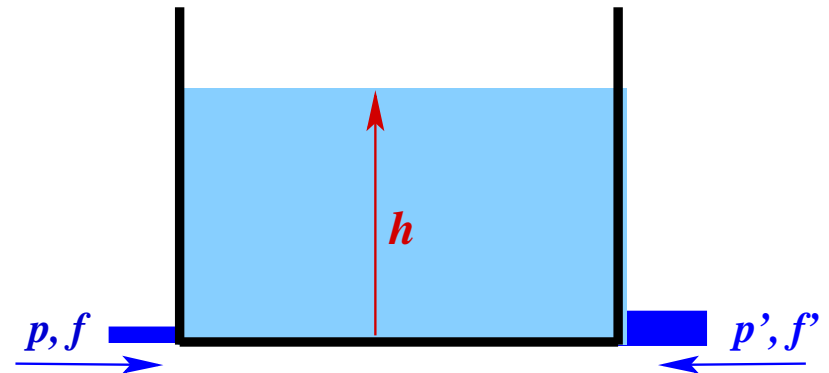
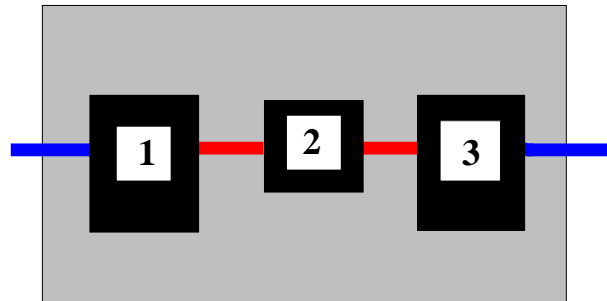


black box 2





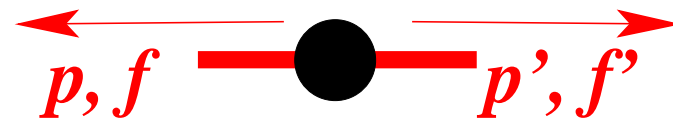
black box 1 & 3



black box 2



interconnections



Black box 1

$$A_1 \frac{d}{dt} h_1 = f_1 + f'_1$$

$$B_1 f_1 = \begin{cases} \sqrt{|p_1 - p_0 - \rho h_1|} & \text{if } p_1 - p_0 \geq \rho h_1 \\ -\sqrt{|p_1 - p_0 - \rho h_1|} & \text{if } p_1 - p_0 \leq \rho h_1 \end{cases}$$

$$C f'_1 = \begin{cases} \sqrt{|p'_1 - p_0 - \rho h_1|} & \text{if } p'_1 - p_0 \geq \rho h_1 \\ -\sqrt{|p'_1 - p_0 - \rho h_1|} & \text{if } p'_1 - p_0 \leq \rho h_1 \end{cases}$$

Black box 2

$$f_2 = -f'_2, \quad p_2 - p'_2 = \alpha f_2$$

Black box 3

$$A_3 \frac{d}{dt} h_3 = f_3 + f'_3$$

$$C f_3 = \begin{cases} \sqrt{|p_3 - p_0 - \rho h_3|} & \text{if } p_3 - p_0 \geq \rho h_3 \\ -\sqrt{|p_3 - p_0 - \rho h_3|} & \text{if } p_3 - p_0 \leq \rho h_3 \end{cases}$$

$$C_3 f'_3 = \begin{cases} \sqrt{|p'_3 - p_0 - \rho h_3|} & \text{if } p'_3 - p_0 \geq \rho h_3 \\ -\sqrt{|p'_3 - p_0 - \rho h_3|} & \text{if } p'_3 - p_0 \leq \rho h_3 \end{cases}$$

Interconnection laws

$$p'_1 = p_2, \quad f'_1 + f_2 = 0, \quad p'_2 = p_3, \quad f'_2 + f_3 = 0$$

Variables of interest

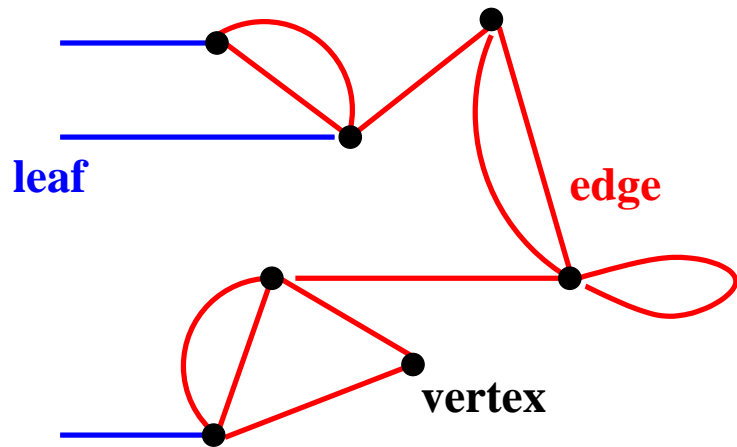
$$p_{\text{left}} = p_1, \quad f_{\text{left}} = f_1, \quad p_{\text{right}} = p'_3, \quad f_{\text{right}} = f'_3$$

Formalization



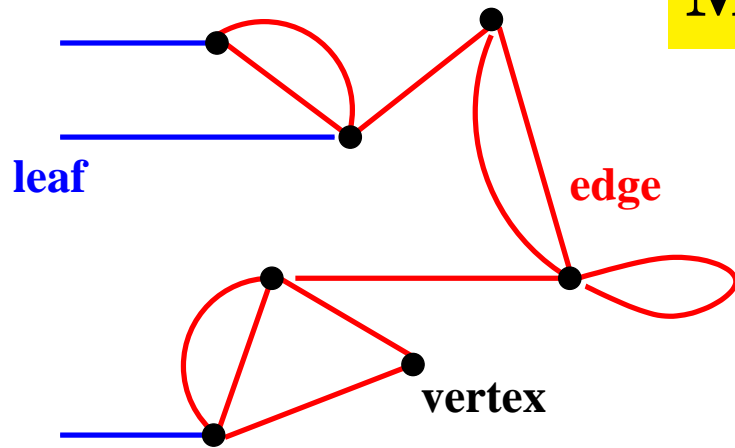
Architecture & module embedding

Architecture

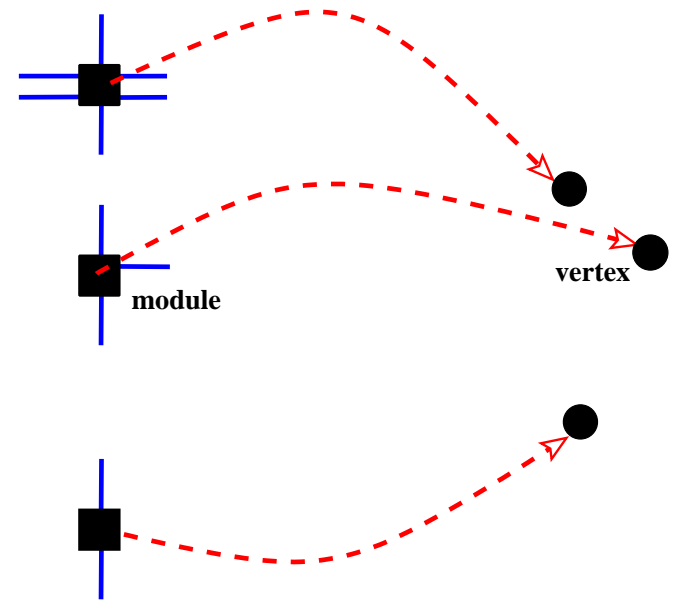


Architecture & module embedding

Architecture

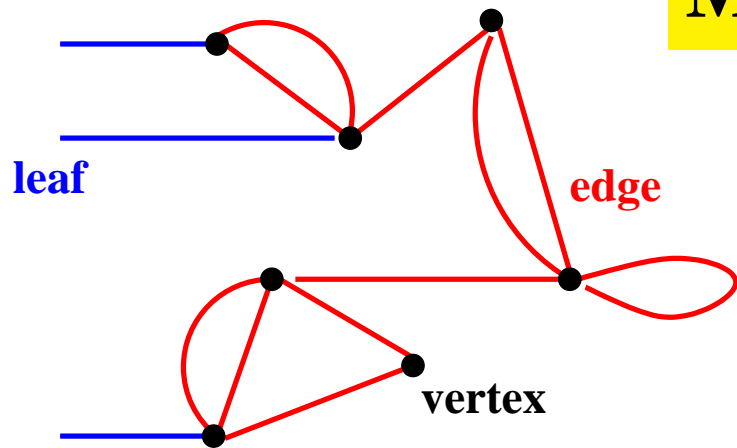


Modules (systems) in the vertices

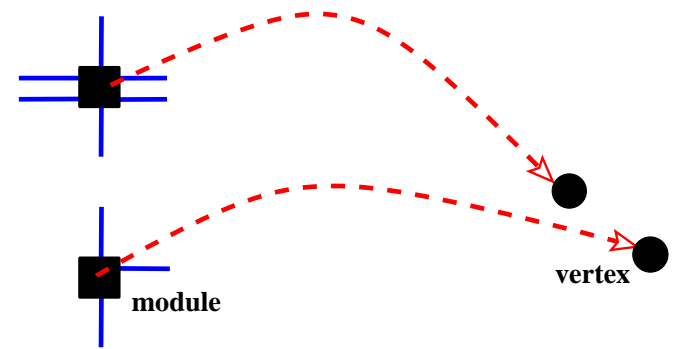


Architecture & module embedding

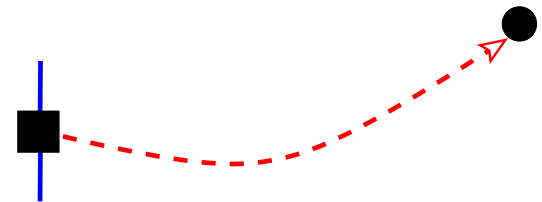
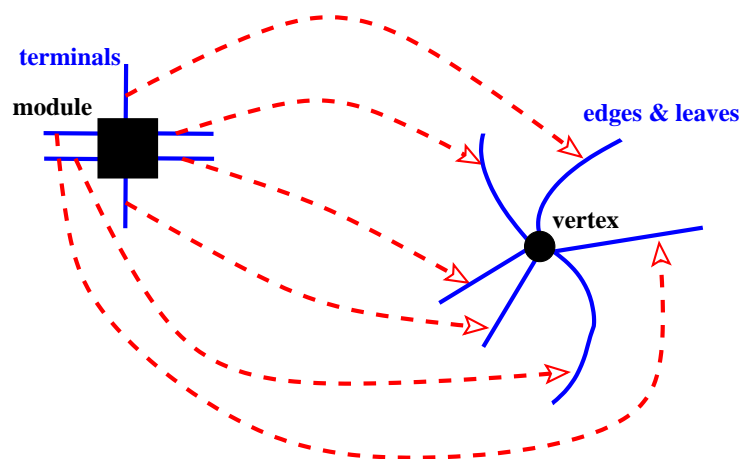
Architecture



Modules (systems) in the vertices



Terminals in the edges



Interconnection architecture

A **graph with leaves** defined as $\mathcal{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, \mathcal{A})$

\mathbb{V} the set of *vertices*,

\mathbb{E} the set of *edges*,

\mathbb{L} the set of *leaves*,

\mathcal{A} the *adjacency map*.

\mathcal{A} associates

with each edge $e \in \mathbb{E}$ an unordered pair

$$\mathcal{A}(e) = [v_1, v_2] \quad v_1, v_2 \in \mathbb{V},$$

with each leaf $\ell \in \mathbb{L}$ an element $\mathcal{A}(\ell) = v \in \mathbb{V}$.

Module embedding

The *module embedding* associates
a module with each vertex,
a $1 \leftrightarrow 1$ assignment between the
edges and leaves adjacent to the vertex and
the terminals of the module.

Module embedding

The ***module embedding*** associates a module with each vertex, a $1 \leftrightarrow 1$ assignment between the edges and leaves adjacent to the vertex and the terminals of the module.

Vertices specify the subsystems,
edges how terminals of subsystems are connected,
leaves how the interconnected system interacts with the environment.

Module embedding

Vertices \rightsquigarrow **Subsystems**

Edges \rightsquigarrow **Interconnections**

Manifest variables

The *manifest variable assignment* is a map that assigns the manifest variables as a function of the terminal (or, more general, the module) variables.

The terminal variables are henceforth considered as latent variables.

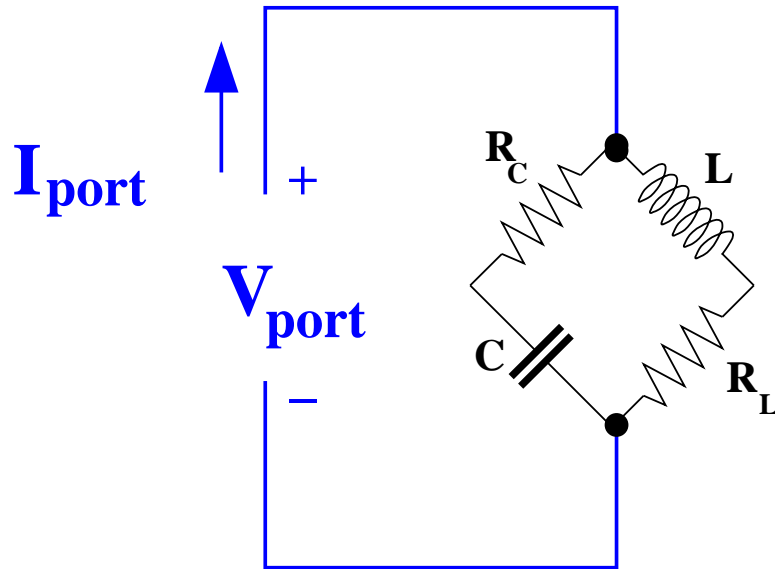
Behavioral equations

1. **Module equations** for each vertex.
Relation among the variables on the terminals of the subsystems.
2. **Interconnection equations** for each edge.
Equating the variables on the terminals associated with the same edge.
3. **Manifest variable assignment**
Specifies the variables of interest.

A very classical example

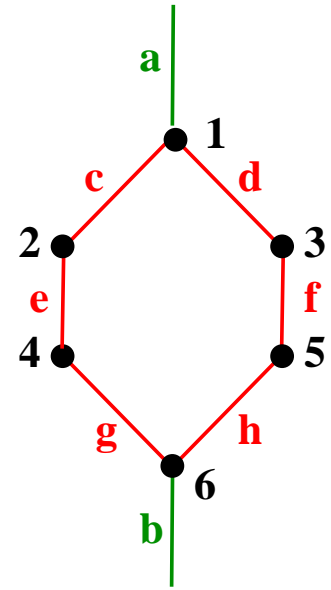
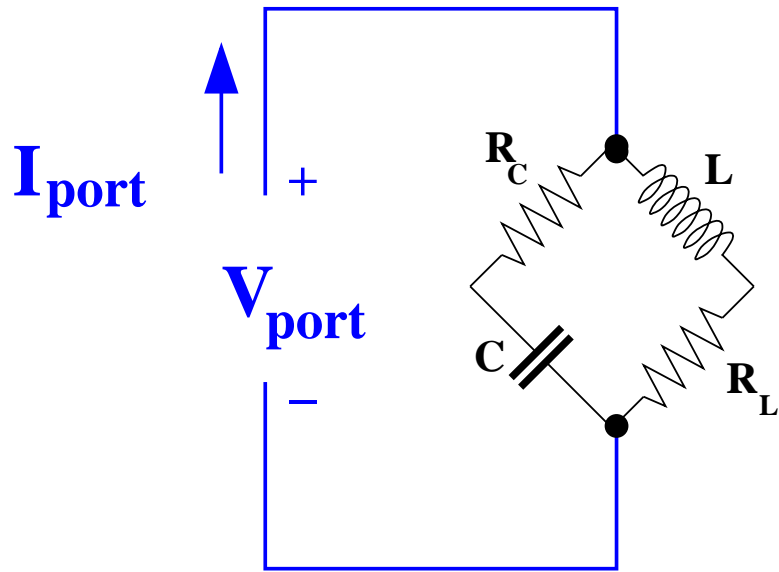


RLC circuit

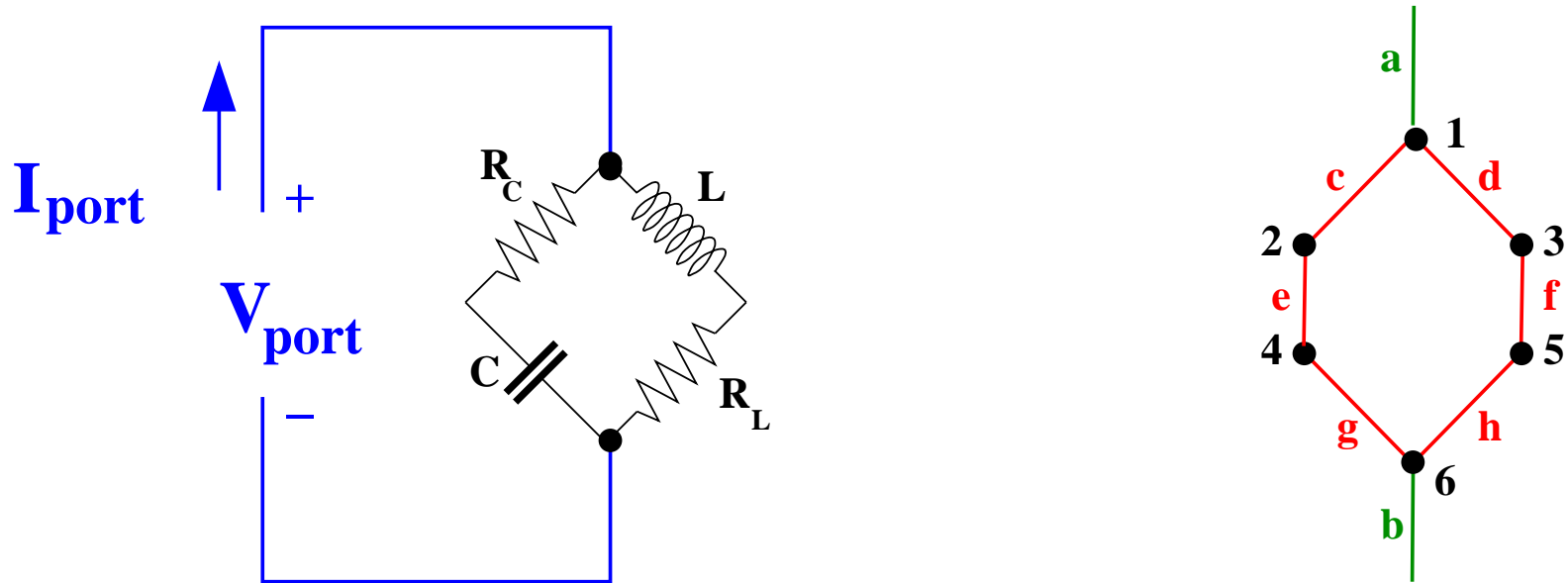


!!! Model the port behavior !!!

RLC circuit



RLC circuit



$$R_C \mapsto 2, R_L \mapsto 5, C \mapsto 4, L \mapsto 3, \text{connector}_1 \mapsto 1, \text{connector}_2 \mapsto 6,$$

$$1_{R_C} \mapsto c, 2_{R_C} \mapsto e, 1_{R_L} \mapsto f, 2_{R_L} \mapsto h, 1_C \mapsto e, 2_C \mapsto g, 1_L \mapsto d, 2_L \mapsto f,$$

$$1_{\text{connector}_1} \mapsto a, 2_{\text{connector}_1} \mapsto c, 3_{\text{connector}_1} \mapsto d,$$

$$1_{\text{connector}_2} \mapsto b, 2_{\text{connector}_2} \mapsto g, 3_{\text{connector}_2} \mapsto h.$$

Module equations

vertex 1

$$V_{1_{\text{connector}_1}} = V_{2_{\text{connector}_1}} = V_{3_{\text{connector}_1}},$$

$$I_{1_{\text{connector}_1}} + I_{2_{\text{connector}_1}} + I_{3_{\text{connector}_1}} = 0;$$

vertex 2

$$V_{1_{R_C}} - V_{2_{R_C}} = R_C I_{1_{R_C}}, \quad I_{1_{R_C}} + I_{2_{R_C}} = 0;$$

vertex 3

$$L \frac{d}{dt} I_{I_L} = V_{1_L} - V_{2_L}, \quad I_{1_L} + I_{2_L} = 0;$$

vertex 4

$$C \frac{d}{dt} (V_{1_C} - V_{2_C}) = I_{1_C}, \quad I_{1_C} + I_{2_C} = 0;$$

vertex 5

$$V_{1_{R_L}} - V_{2_{R_L}} = R_L I_{1_{R_L}}, \quad I_{1_{R_L}} + I_{2_{R_L}} = 0;$$

vertex 6

$$V_{1_{\text{connector}_2}} = V_{2_{\text{connector}_2}} = V_{3_{\text{connector}_2}},$$

$$I_{1_{\text{connector}_2}} + I_{2_{\text{connector}_2}} + I_{3_{\text{connector}_2}} = 0.$$

Interconnection equations

edge c

$$V_{1_{RC}} = V_{2_{\text{connector}_1}}, I_{1_{RC}} + I_{2_{\text{connector}_1}} = 0;$$

edge d

$$V_{1_L} = V_{3_{\text{connector}_1}}, I_{1_L} + I_{3_{\text{connector}_1}} = 0;$$

edge e

$$V_{2_{RC}} = V_{1_C}, I_{2_{RC}} + I_{1_C} = 0;$$

edge f

$$V_{2_L} = V_{1_{RC}}, I_{2_L} + I_{1_{RC}} = 0;$$

edge g

$$V_{2_C} = V_{1_{\text{connector}_2}}, I_{2_C} + I_{1_{\text{connector}_2}} = 0;$$

edge h

$$V_{2_{RL}} = V_{2_{\text{connector}_2}}, I_{2_{RL}} + I_{2_{\text{connector}_2}} = 0.$$

Manifest variable assignment

$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

Manifest variable assignment

$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

The module equations

+ the interconnection constraints

+ the manifest variable assignment

form the complete model for the behavior of

$$(V_{\text{external port}}, I_{\text{external port}})$$

Prevalence of latent variables \rightsquigarrow elimination theory.

Manifest variable assignment

$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

Behavior = all

$$(V_{\text{external port}}, I_{\text{external port}}) : \mathbb{R} \rightarrow \mathbb{R}^2$$

$\exists \dots, V_{1_{R_c}}, \dots, I_{3_{\text{connector}_2}} \mathbb{R} \rightarrow \mathbb{R}^{\dots}$ **such that ...**

Manifest behavior

\rightsquigarrow the dynamical system $\Sigma = (\mathbb{R}, \mathbb{R}^2, \mathcal{B})$ with behavior \mathcal{B} specified by:

Case 1: $CR_C \neq \frac{L}{R_L}$

$$\left(\frac{R_C}{R_L} + \left(1 + \frac{R_C}{R_L} \right) CR_C \frac{d}{dt} + CR_C \frac{L}{R_L} \frac{d^2}{dt^2} \right) V = \left(1 + CR_C \frac{d}{dt} \right) \left(1 + \frac{L}{R_L} \frac{d}{dt} \right) R_C I$$

Case 2: $CR_C = \frac{L}{R_L}$

$$\left(\frac{R_C}{R_L} + CR_C \frac{d}{dt} \right) V = (1 + CR_C) \frac{d}{dt} R_C I$$

\rightsquigarrow behavior $\mathcal{B} =$ all solutions $(V, I) : \mathbb{R} \rightarrow \mathbb{R}^2$

Other methodologies

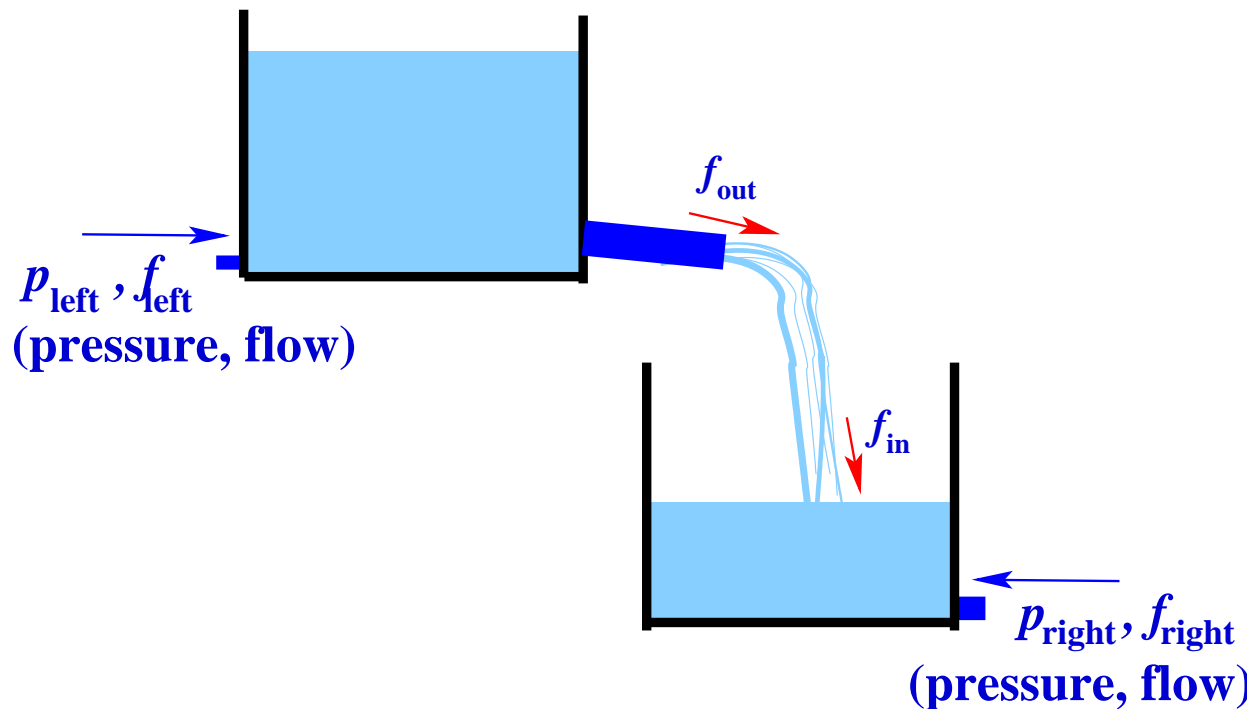


Signal flow graphs



input/output thinking

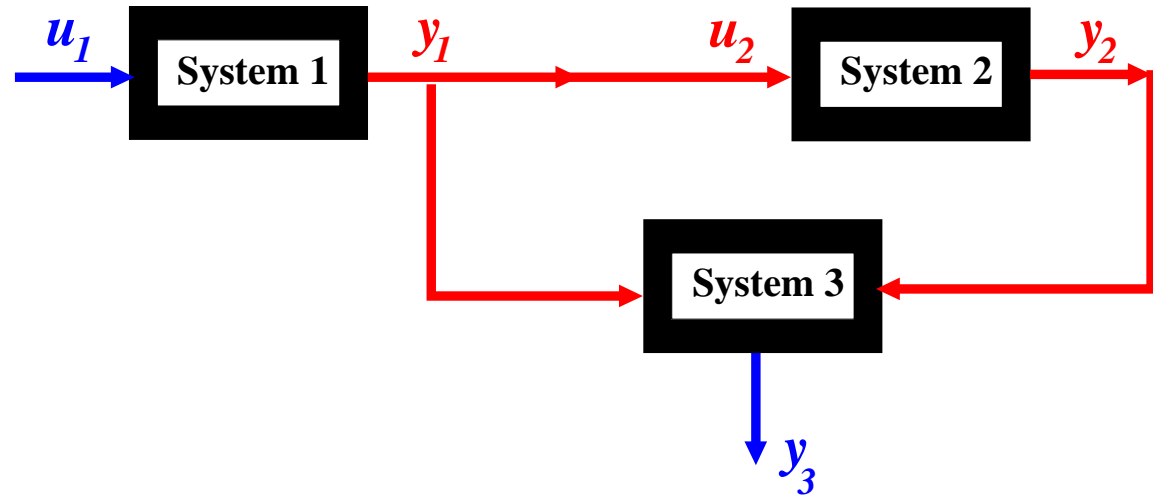
There are many many examples where
output-to-input connection is eminently natural:



input/output thinking



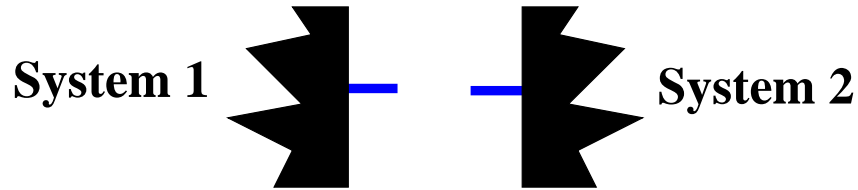
(a)



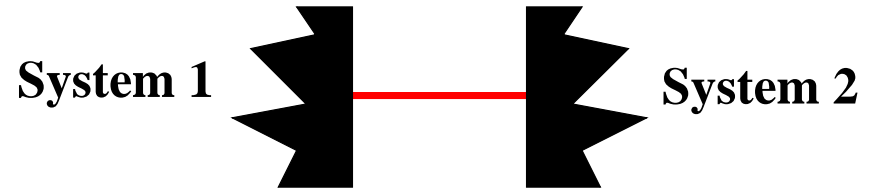
(b)

- shows terminal variables separate
- suggests that inputs and outputs occur at different points
- allows impossible input-output connections

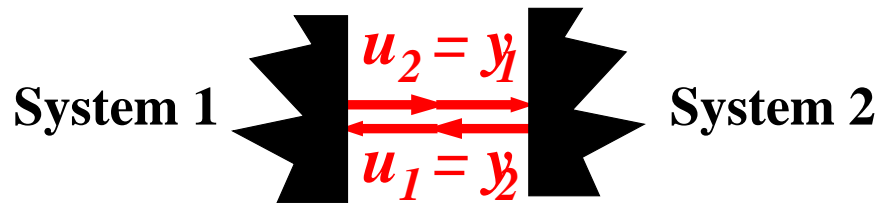
input/output thinking



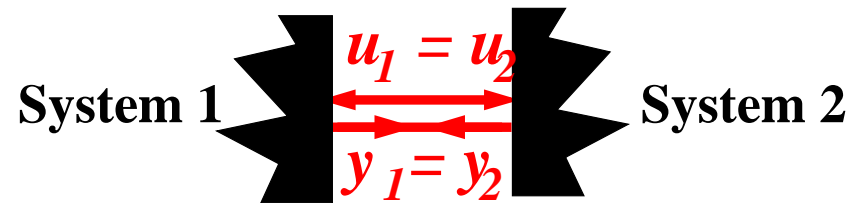
(a)



(b)



(c)



(d)

For physical systems

input-to-input & **output-to-output**

assignment very prevalent.

Physical systems are not signal processors.

input/output thinking

“Block diagrams unsuitable for serious physical modeling

- the control/physics barrier”

“Behavior based (declarative) modeling is a good alternative”



from K.J. Åström, *Present Developments in Control Applications*



**IFAC 50-th Anniversary Celebration
Heidelberg, September 12, 2006.**

Bond graphs



Bond graphs

Interconnection variables:

a **flow** and an **effort**

product = power

- **current & voltage**
- **velocity & force**
- **mass flow & pressure**
- **heat flow & temperature**
 $\frac{\text{heat flow}}{\text{temperature}}$ & temperature
- ...

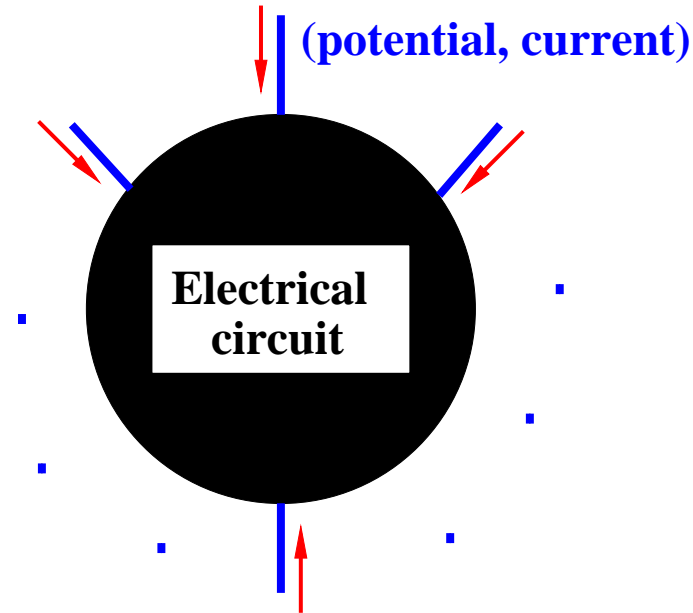
Bond graphs

Interconnection variables:

a **flow** and an **effort** **product = power**

- 1. Mechanical interconnections equate positions, not velocities**
- 2. Not all interconnections involve equating energy transfer**
- 3. Terminals are for interconnection, ports are for energy transfer**

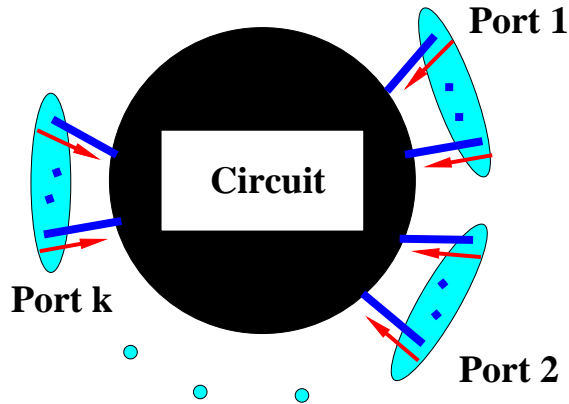
Terminals versus ports



Terminal variables and behavior:

$$(V_1, I_1, V_2, I_2, \dots, V_n, I_n) \rightsquigarrow \text{behavior } \mathcal{B} \subseteq \left(\mathbb{R}^{2n} \right)^{\mathbb{R}}$$

Terminals versus ports



Port $:\Leftrightarrow$ **sum currents = 0**
potentials + constant \Rightarrow potentials

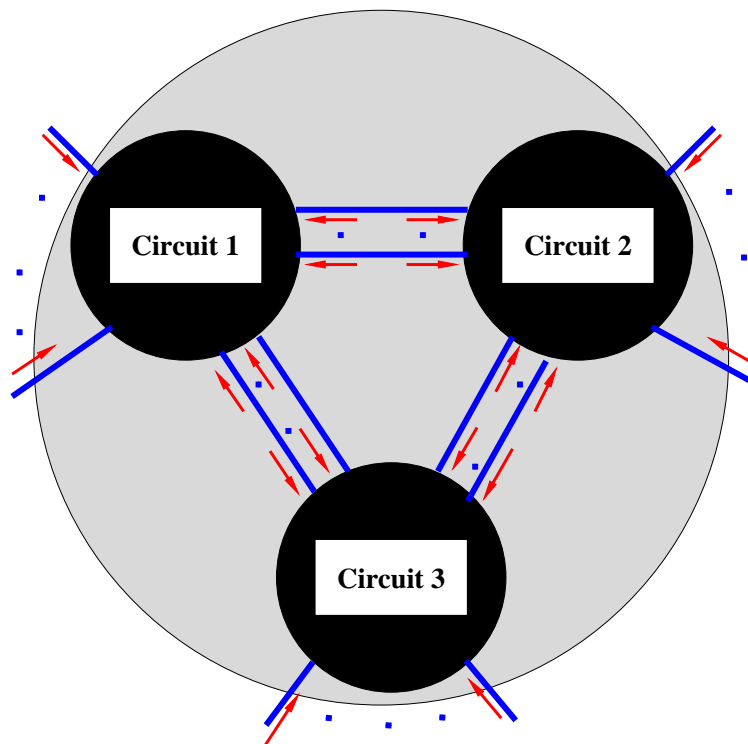
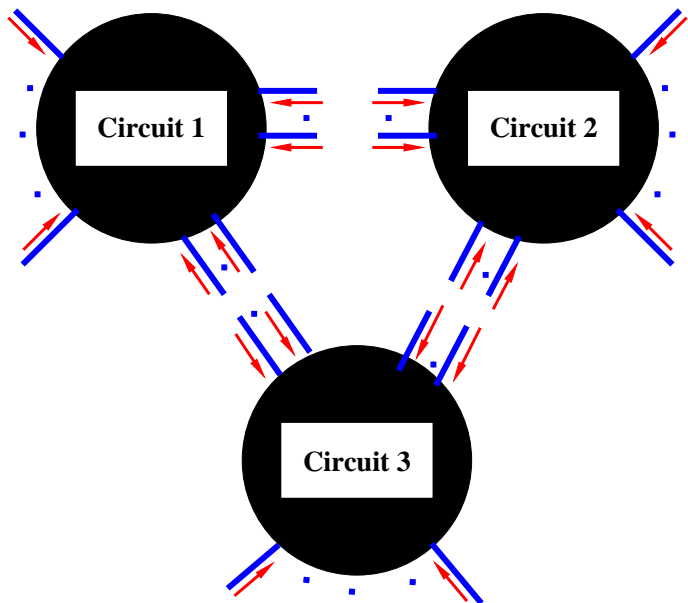
$$\left(\boxed{V_1, I_1, \dots, V_p, I_p}, V_{p+1}, \dots, I_n \right) \in \mathcal{B}, \alpha : \mathbb{R} \rightarrow \mathbb{R}$$

\Downarrow

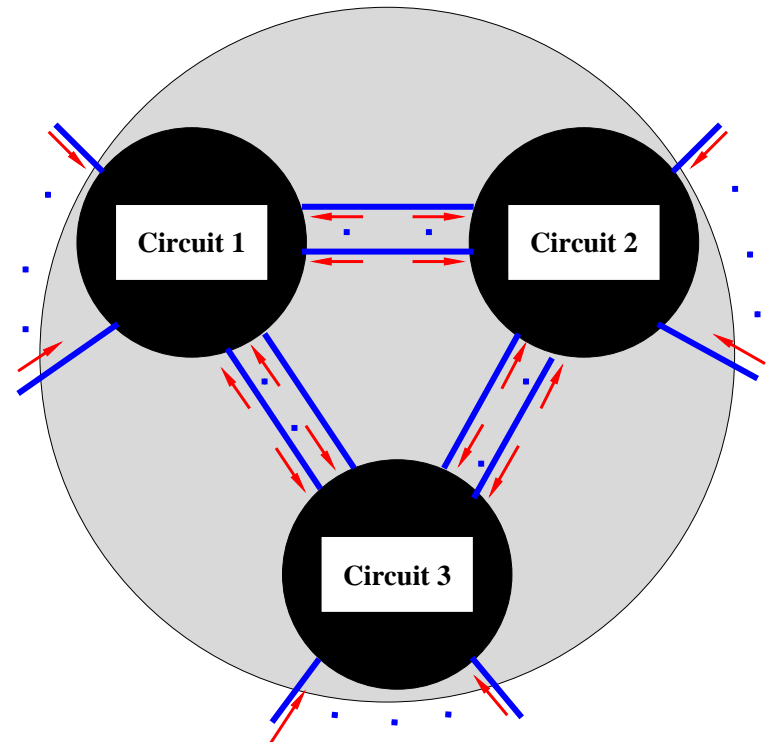
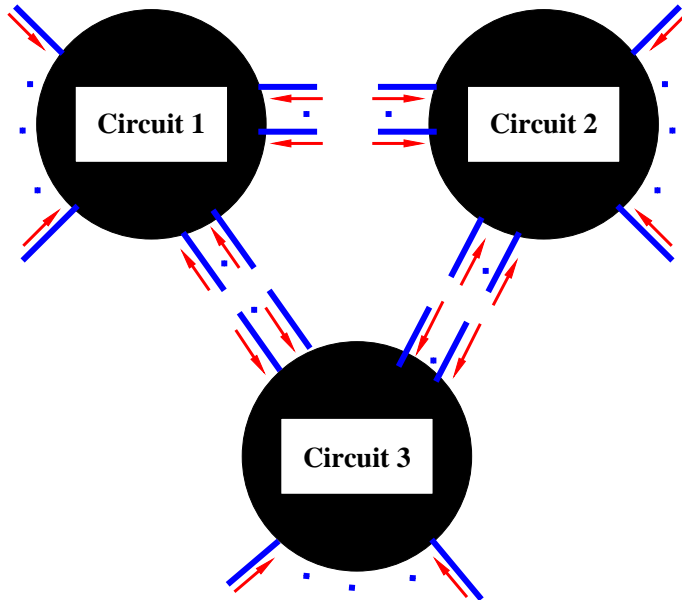
$$\left(\boxed{V_1 + \alpha, I_1, \dots, V_p + \alpha, I_p}, V_{p+1}, \dots, I_n \right) \in \mathcal{B}$$

$$\boxed{I_1 + \dots + I_p} = 0$$

Terminals versus ports



Terminals versus ports



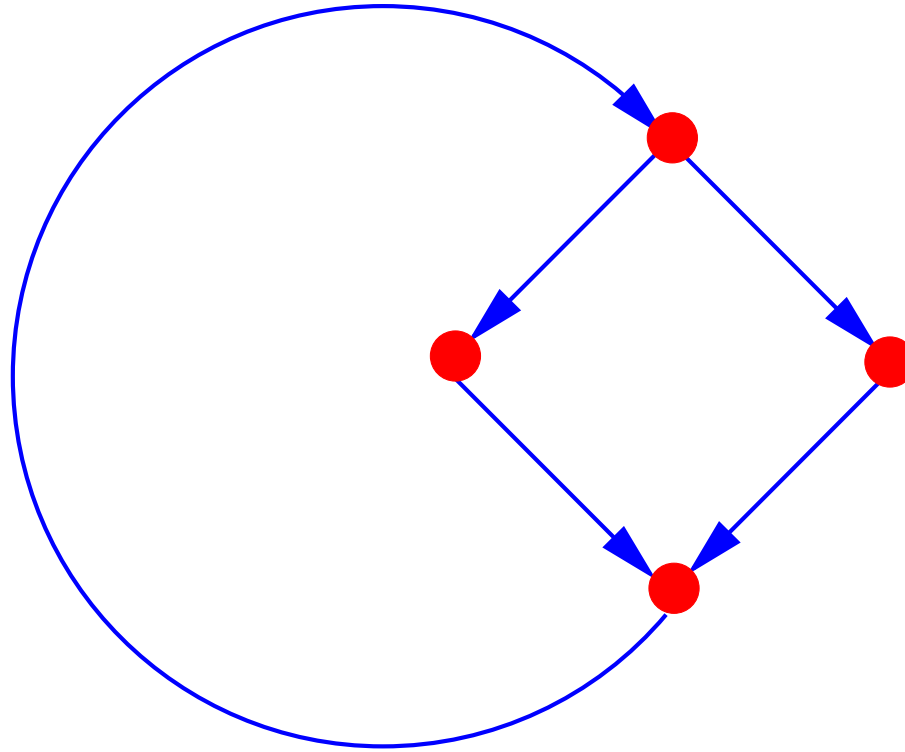
Interconnection via terminals, energy transfer via ports; one cannot talk about

“the energy transferred from circuit 1 to circuit 2”

Circuit diagrams



Circuit diagrams



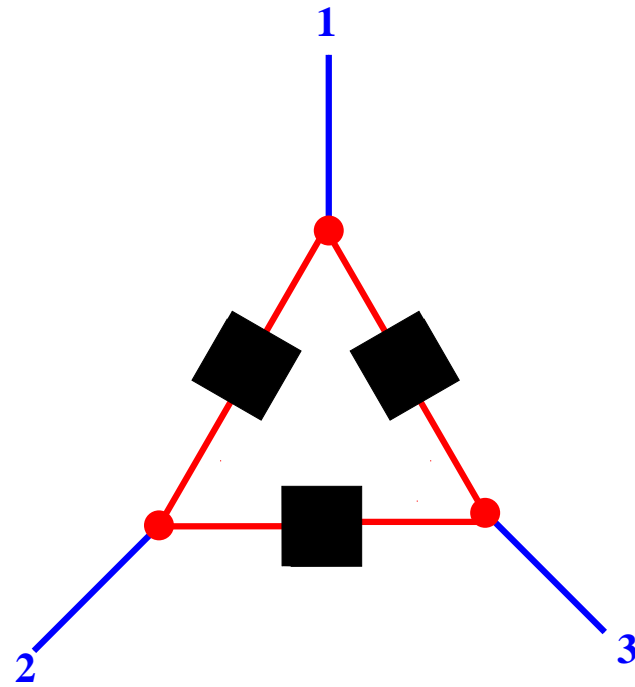
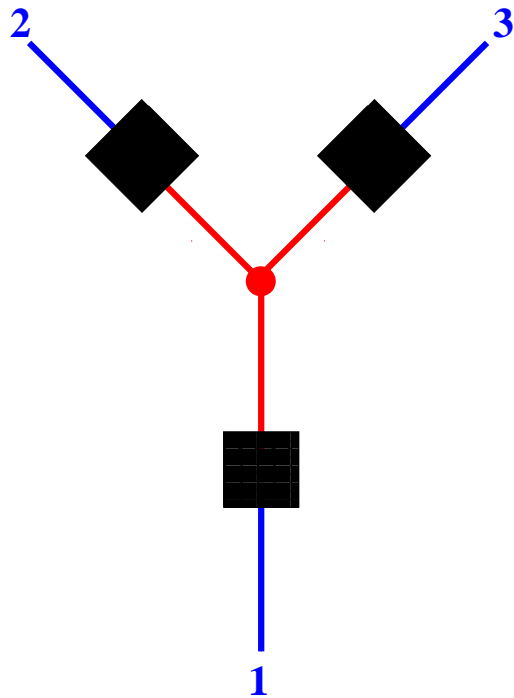
Circuit diagrams with

nodes & branches & KVL & KCL

are only effective with 2-terminal 1-ports.

Circuit diagrams

Not closed under composition



Various facets of control

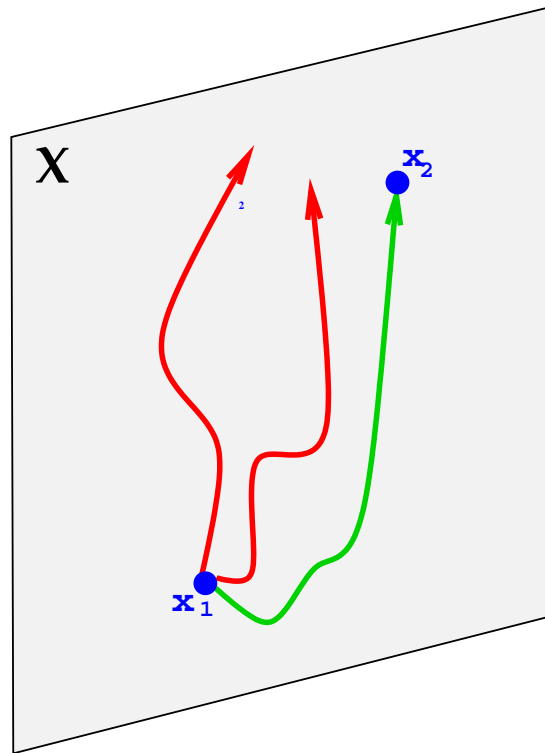


Path planning

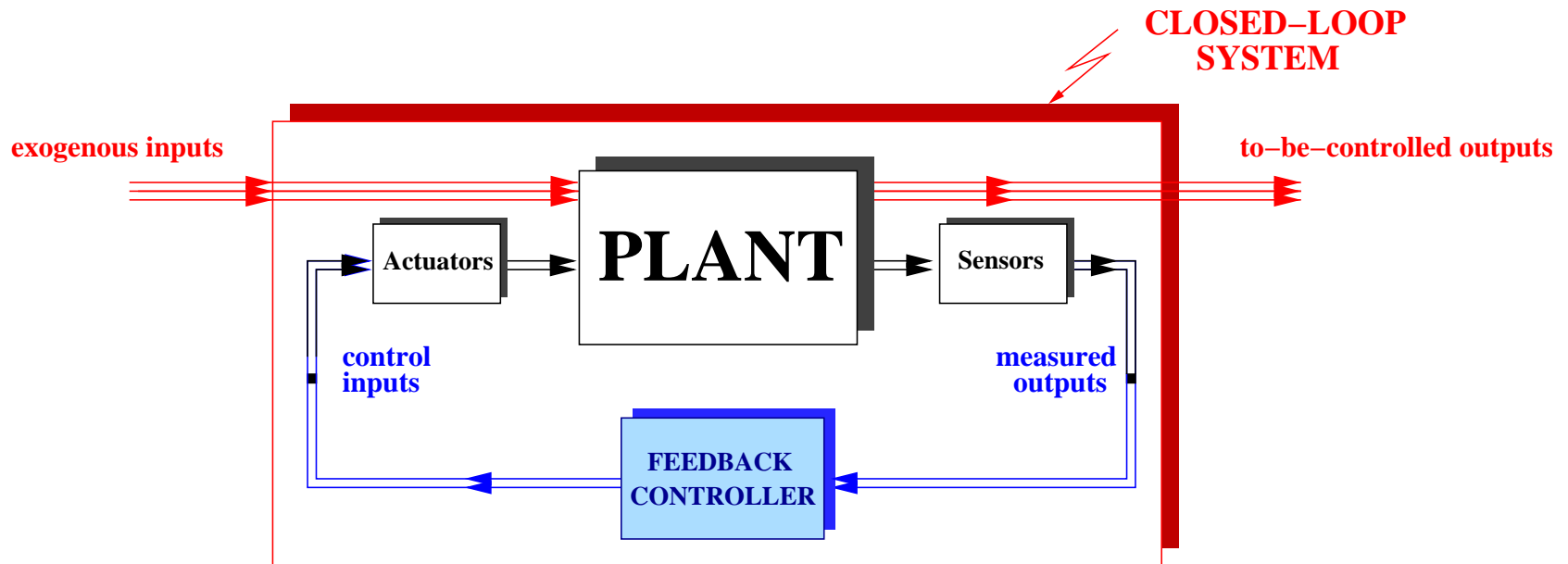
$$\frac{d}{dt}x = f(x, u)$$

Choose time-function $u(\cdot) : [0, T] \rightarrow \mathbb{U}$ so as to achieve (optimal) state transfer.

‘open loop control’



Decision making



Choose **map from sensor outputs to actuator inputs** so as to achieve good (optimal) performance.

‘feedback control’

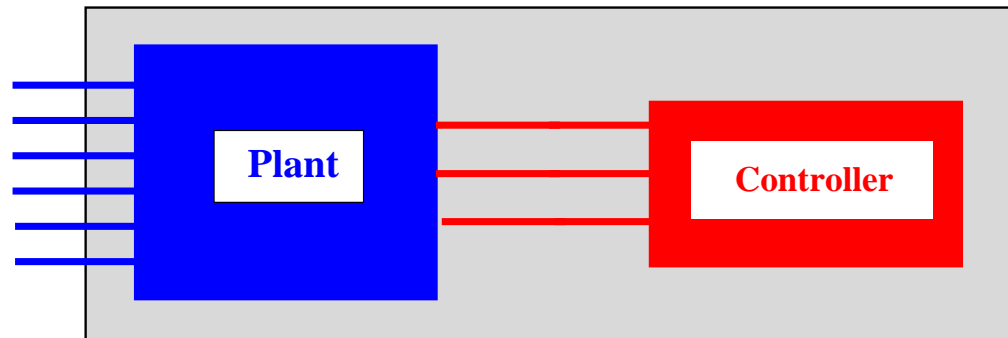
‘closed loop control’

‘intelligent control’

Embedded control



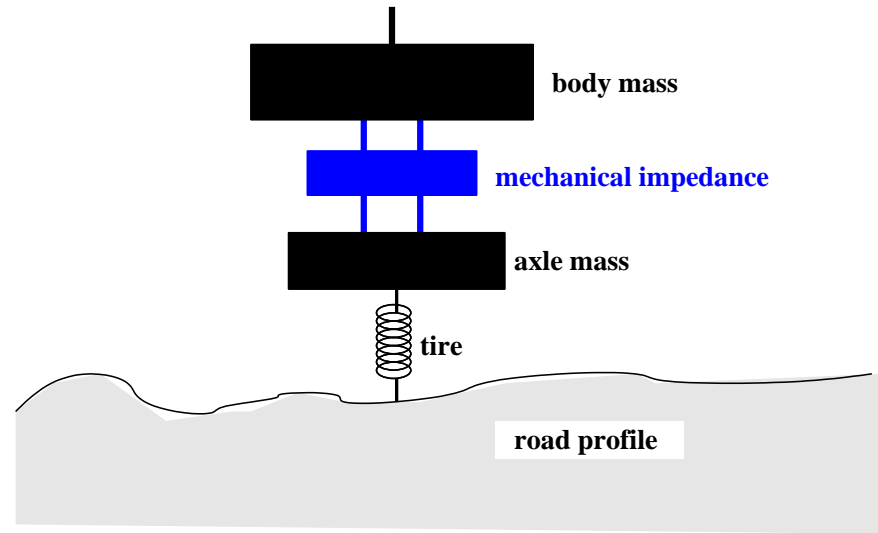
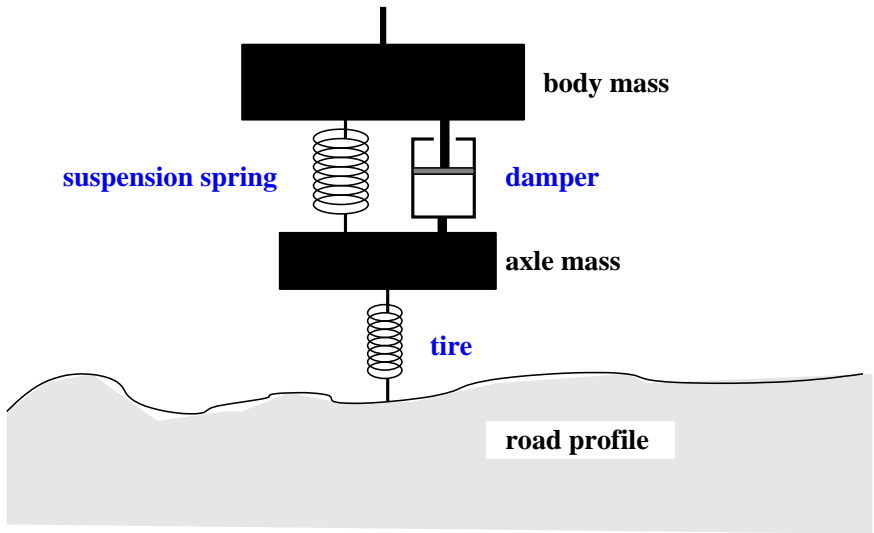
Embedded systems



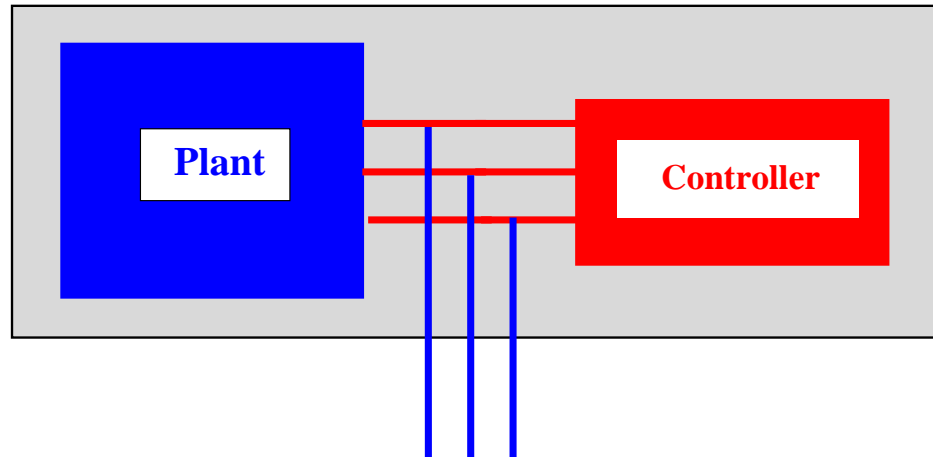
Choose **controller** so as to achieve good (optimal) performance of the interconnected system

‘control as interconnection’
‘integrated system design’

Example

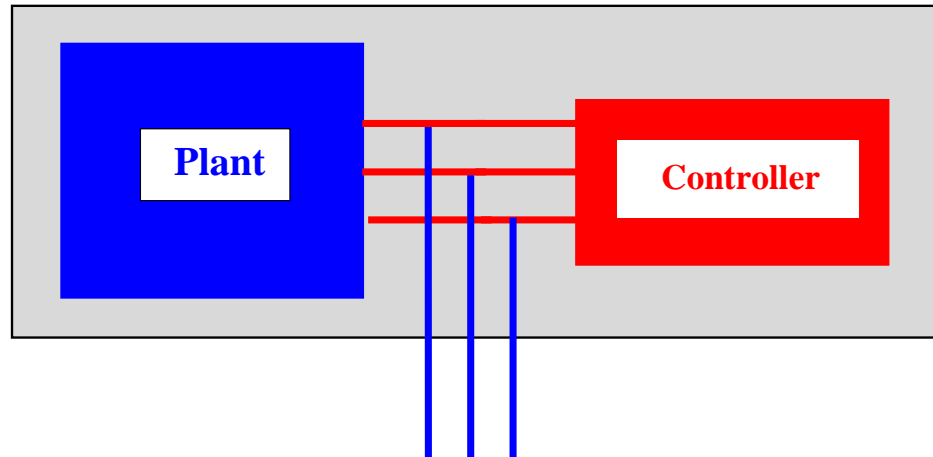


Control as interconnection



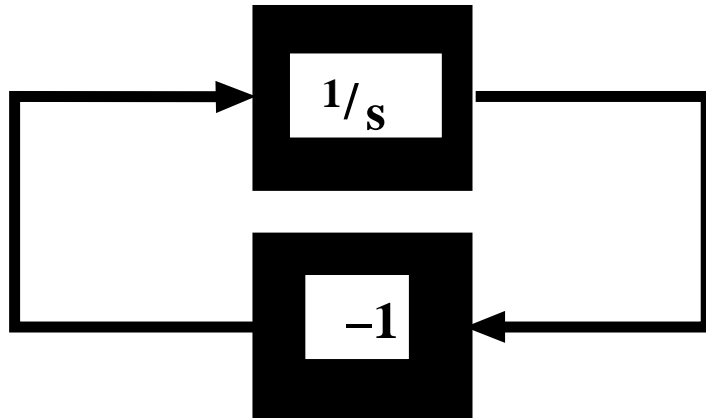
**Plant behavior \mathcal{P} , controller behavior \mathcal{K} ,
controlled behavior $\mathcal{P} \cap \mathcal{K}$.**

Control as interconnection

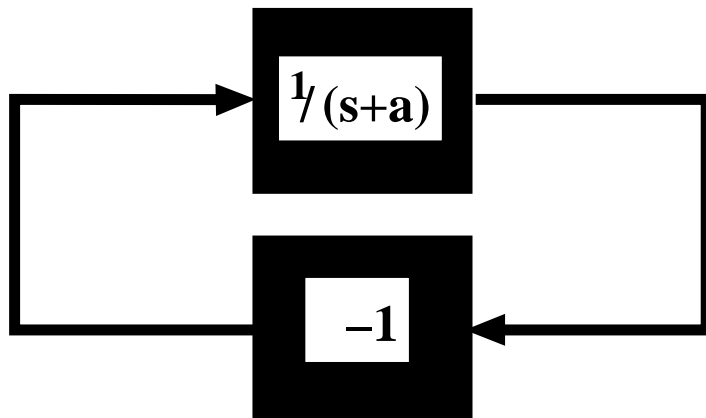


**Plant behavior \mathcal{P} , controller behavior \mathcal{K} ,
controlled behavior $\mathcal{P} \cap \mathcal{K}$.**

Robustness



$$\frac{d}{dt}y + y = 0$$



$$\frac{d}{dt}y + (1 + a)y = 0$$

Robust stability, but $\left\| \frac{1}{s} - \frac{1}{s+a} \right\| = \infty$.

Robustness

Viewing plant as a behavior, rather than i/o map \rightsquigarrow

Robustness: Given \mathcal{P} , stabilized by \mathcal{K} , how close to \mathcal{P} needs \mathcal{P}' be to be also stabilized by \mathcal{K} ?

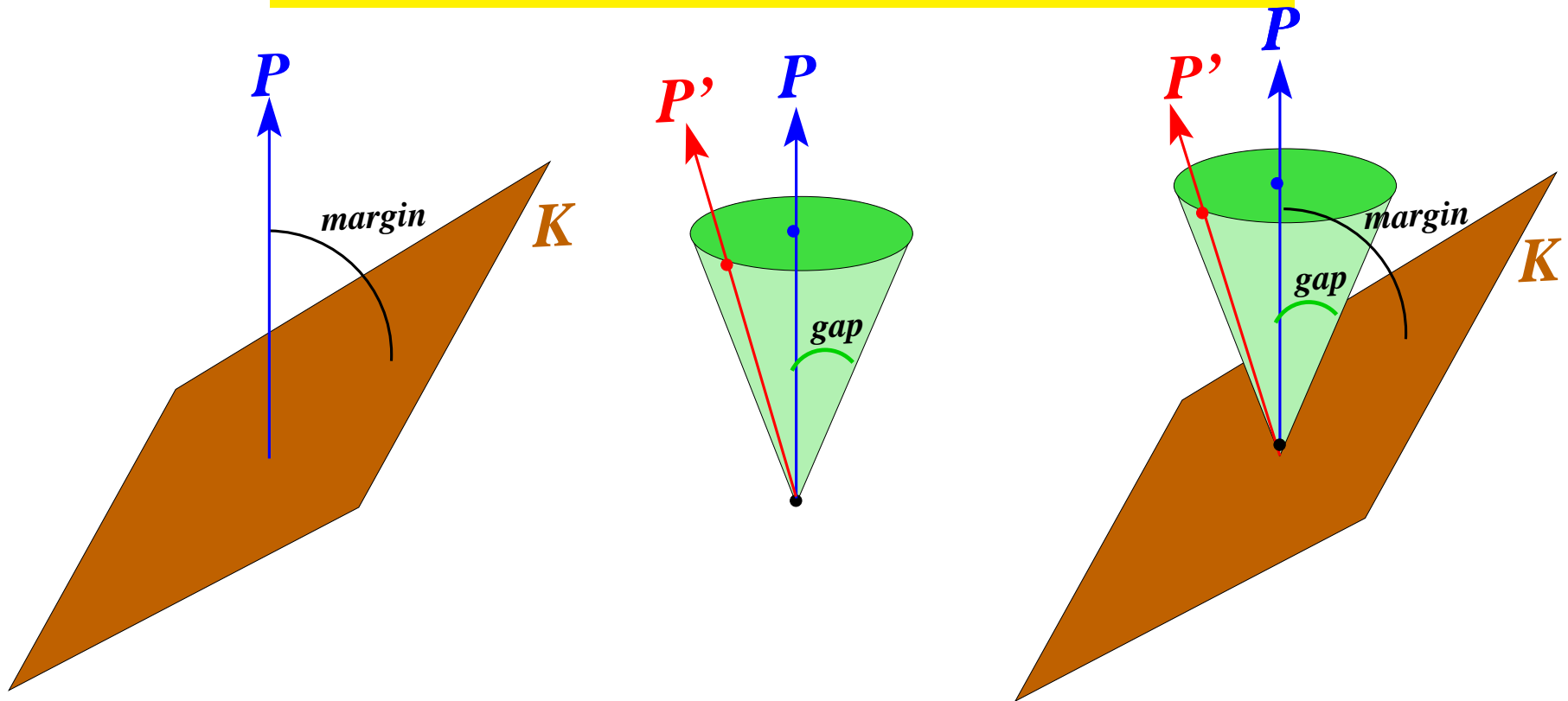
Robustness

Robustness: Given \mathcal{P} , stabilized by \mathcal{K} , how close to \mathcal{P} needs \mathcal{P}' be to be also stabilized by \mathcal{K} ?

$$\text{'gap'}(\mathcal{P}, \mathcal{P}') < \text{'margin'}(\mathcal{P}, \mathcal{K})$$

Robustness

$$\text{'gap'}(\mathcal{P}, \mathcal{P}') < \text{'margin'}(\mathcal{P}, \mathcal{K})$$



Exactly approach used in robust control,

\mathcal{L}_2 -, \mathcal{H}_2 - 'gap', 'v-gap', ...

Overview



Conclusions

- **Interconnection = variable (terminal) sharing**
- **Modeling by physical systems proceeds by tearing, zooming, and linking**
- **Hierarchical procedure**

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Conclusions

- **Interconnection = variable (terminal) sharing**
- **Modeling by physical systems proceeds by tearing, zooming, and linking**
- **Hierarchical procedure**
- **Importance of latent variables and the elimination theorem**
- **Limitations of input/output thinking**
- **The behavioral approach & its view of system interconnection are a pedagogical ‘must’**

Reference: Jan C. Willems

The behavioral approach to open and interconnected systems

Control Systems Magazine, volume 27, pages 46 – 99, 2007

Details & copies of the lecture frames are available from/at

Jan.Willems@esat.kuleuven.be

<http://www.esat.kuleuven.be/~jwillems>

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Thank you

Thank you

Thank you

Thank you

Thank you

Thank you

Thank you

Happy Birthday, Alberto !!!

