TEARING, ZOOMING, and LINKING

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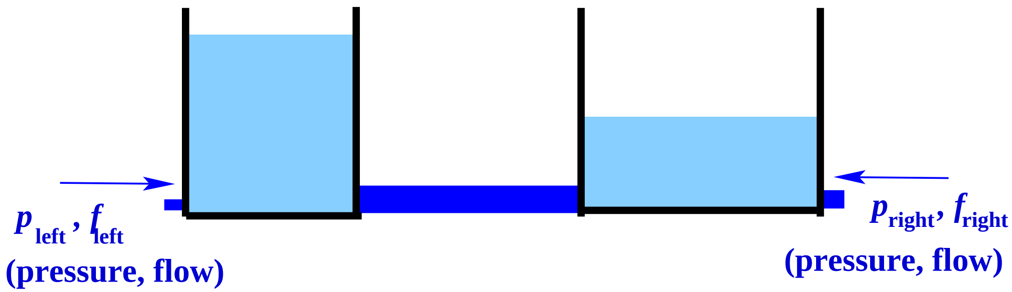
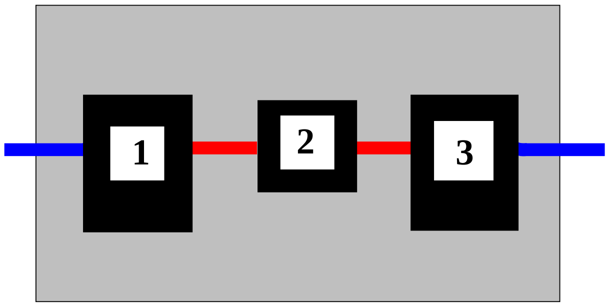
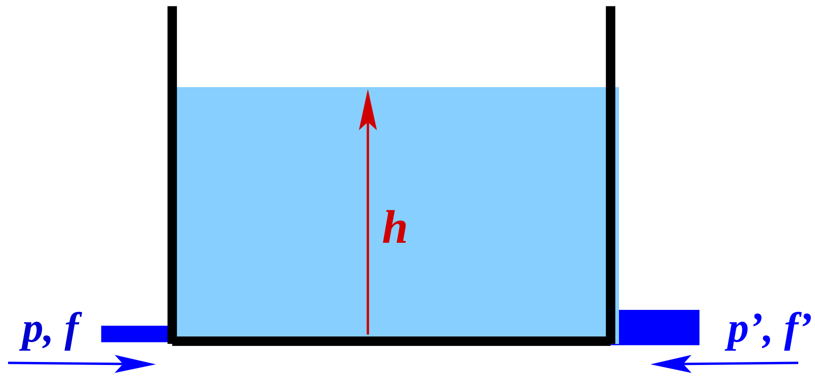
Thanks to

Tommaso Cotroneo & his dissertation

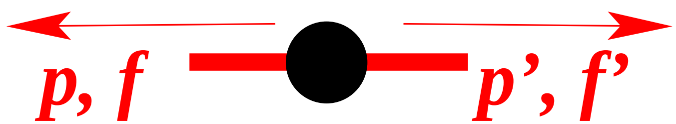

p_{left}, f_{left}
(pressure, flow)
p_{right}, f_{right}
(pressure, flow)


(pressure, flow)
(pressure, flow)


1
2
3


h
p, f
p’, f’


p, f
p’, f’


p, f
p’, f’

$$A_1 \frac{d}{dt} h_1 = f_1 + f_1', \tag{1}$$

$$B_1 f_1 = \begin{cases} \sqrt{|p_1 - p_0 - \rho h_1|} & \text{if } p_1 - p_0 \geq \rho h_1, \\ -\sqrt{|p_1 - p_0 - \rho h_1|} & \text{if } p_1 - p_0 \leq \rho h_1, \end{cases} \tag{2}$$

$$C f_1' = \begin{cases} \sqrt{|p_1' - p_0 - \rho h_1|} & \text{if } p_1' - p_0 \geq \rho h_1, \\ -\sqrt{|p_1' - p_0 - \rho h_1|} & \text{if } p_1' - p_0 \leq \rho h_1, \end{cases} \tag{3}$$

$$f_2 = -f_2', \;\; p_2 - p_2' = \alpha f_2, \tag{4}$$

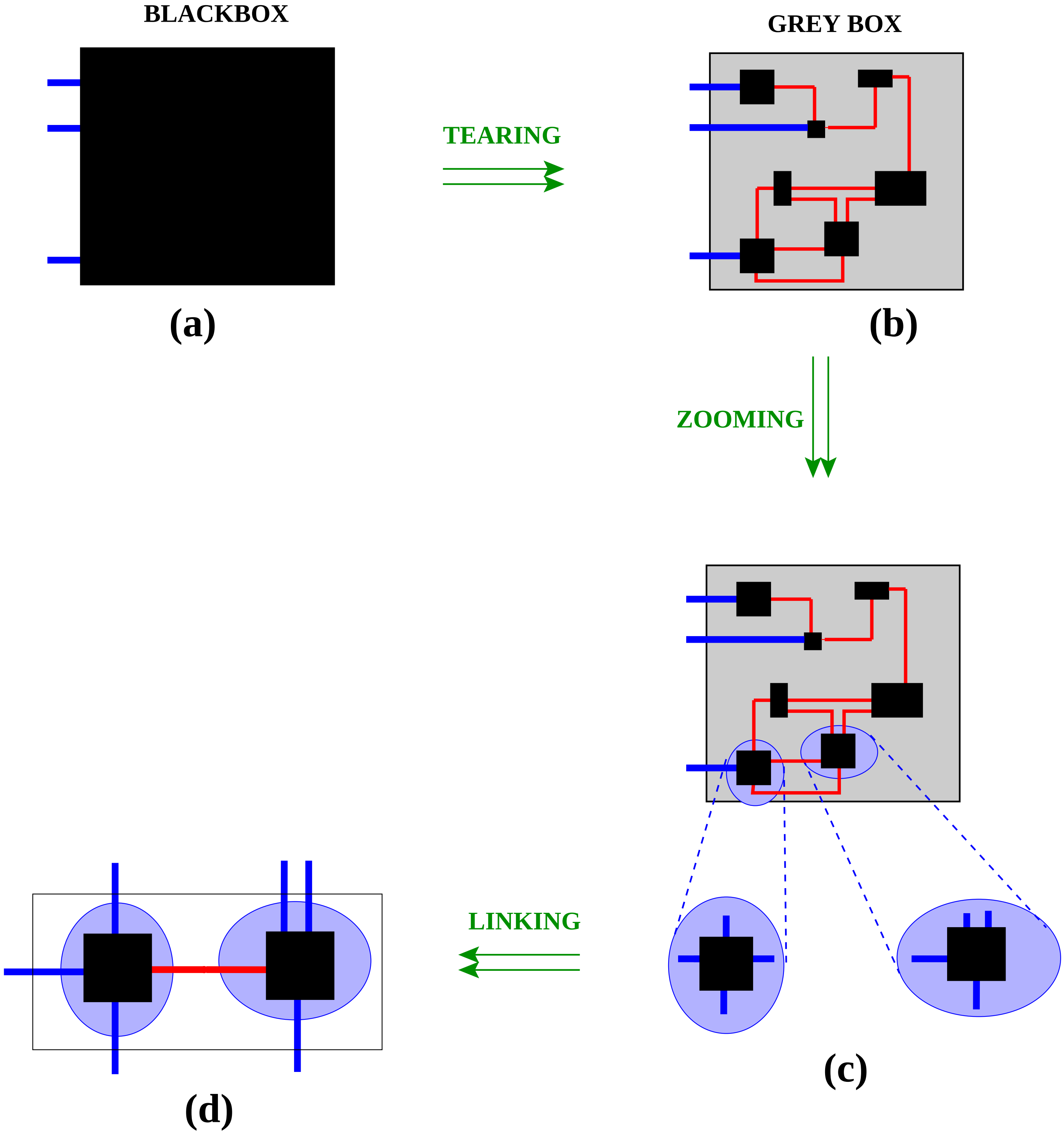
$$A_3 \frac{d}{dt} h_3 = f_3 + f_3', \tag{5}$$

$$C f_3 = \begin{cases} \sqrt{|p_3 - p_0 - \rho h_3|} & \text{if } p_3 - p_0 \geq \rho h_3, \\ -\sqrt{|p_3 - p_0 - \rho h_3|} & \text{if } p_3 - p_0 \leq \rho h_3, \end{cases} \tag{6}$$

$$C_3 f_3' = \begin{cases} \sqrt{|p_3' - p_0 - \rho h_3|} & \text{if } p_3' - p_0 \geq \rho h_3, \\ -\sqrt{|p_3' - p_0 - \rho h_3|} & \text{if } p_3' - p_0 \leq \rho h_3, \end{cases} \tag{7}$$

$$p_1' = p_2, \;\; f_1' + f_2 = 0, \; p_2' = p_3, \;\; f_2' + f_3 = 0, \tag{8}$$

$$p_{\text{left}} = p_1, \; f_{\text{left}} = f_1, \; p_{\text{right}} = p_3', \; f_{\text{right}} = f_3'. \tag{9}$$


BLACKBOX
GREY BOX
TEARING
(a)
(b)
ZOOMING
LINKING
(c)
(d)

Tearing, zooming, linking language

(i) terminals,

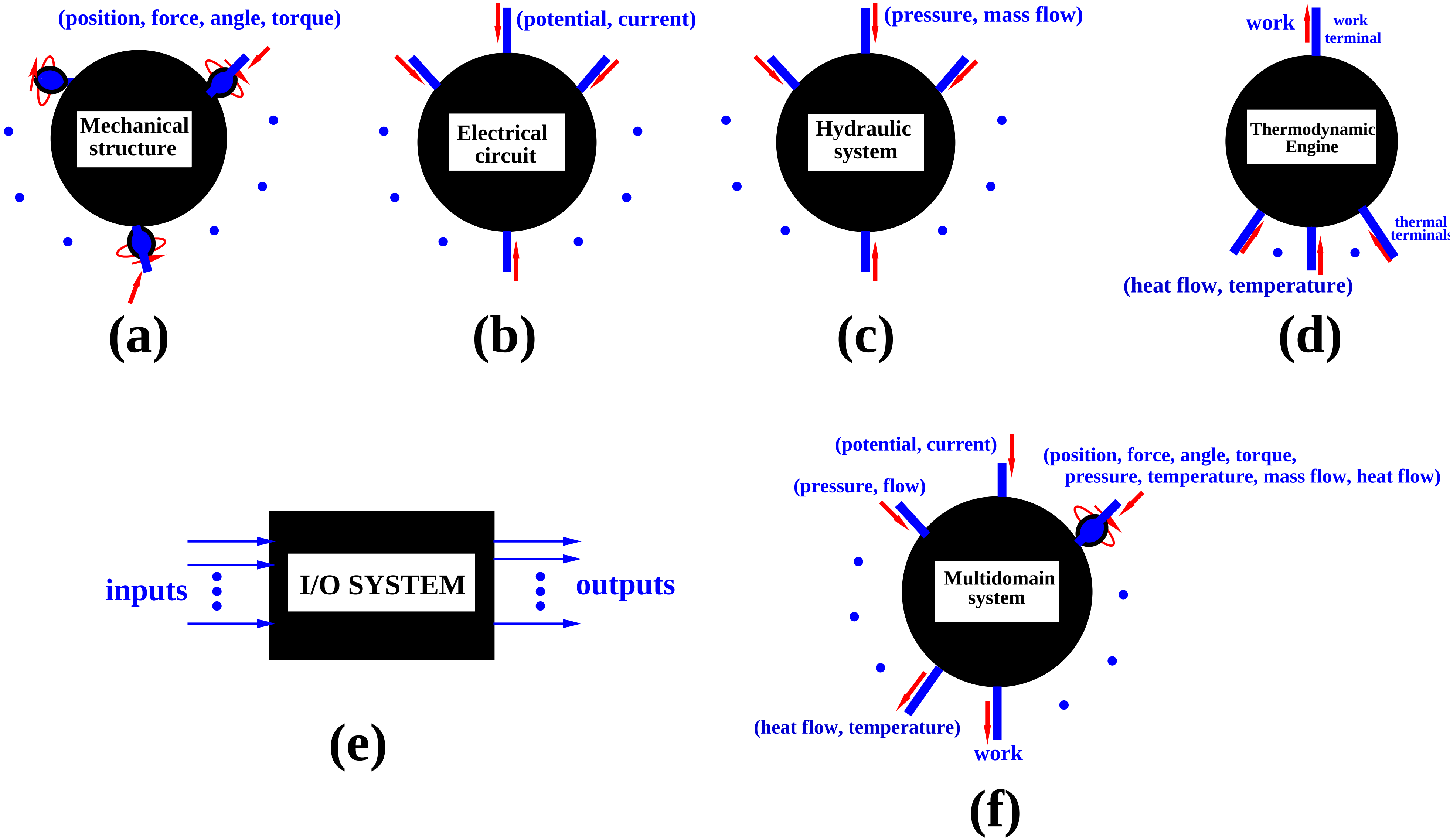
(ii) (parameterized) modules,

(iii) the interconnection architecture,

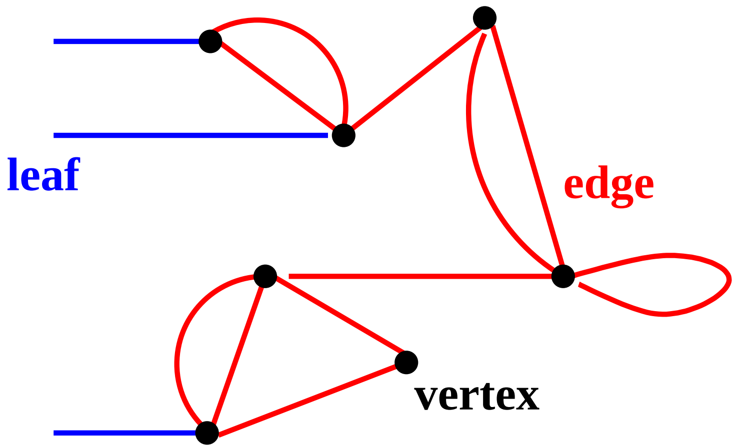
(iv) the module embedding, and

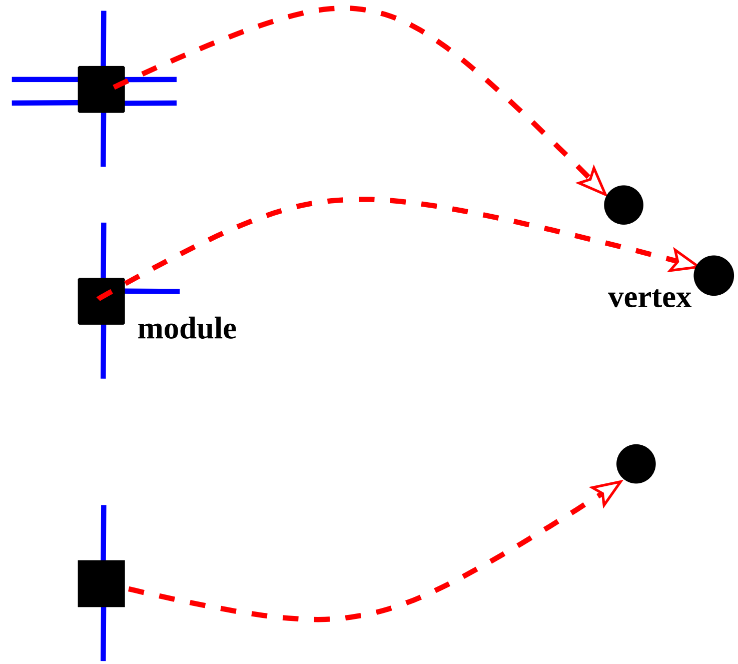
(v) the manifest variable assignment.

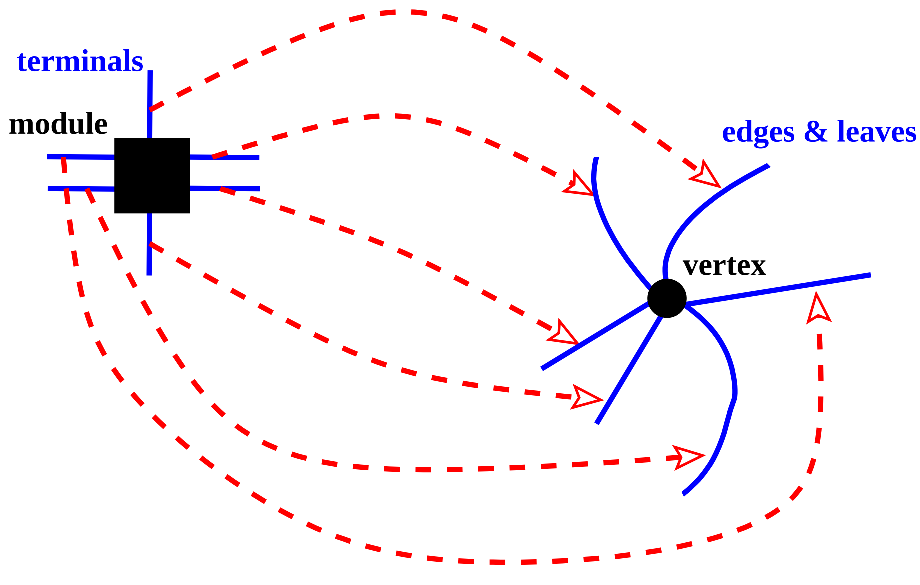
Terminals and Modules



Architecture







Interconnection architecture

A *graph with leaves* defined as $\mathcal{G} = (\mathbb{V}, \mathbb{E}, \mathbb{L}, \mathcal{A})$

$\mathbb{V}$ the set of *vertices*,

$\mathbb{E}$ the set of *edges*,

$\mathbb{L}$ the set of *leaves*,

and $\mathcal{A}$ the *adjacency map*.

$\mathcal{A}$ associates with each edge $e \in \mathbb{E}$

unordered pair $\mathcal{A}(e) = [v_1, v_2] \quad v_1, v_2 \in \mathbb{V}$,

and with each leaf $\ell \in \mathbb{L}$ an element $\mathcal{A}(\ell) = v \in \mathbb{V}$.

Module embedding

The *module embedding* associates
a module with each vertex,
and a $1 \leftrightarrow 1$ assignment between the
edges and leaves adjacent to the vertex and the
terminals of the module.

The edges specify how terminals of subsystems are connected,
and the leaves the interaction with the environment.

Module embedding

Vertices $\rightsquigarrow$ Subsystems

Edges $\rightsquigarrow$ Interconnections

Manifest variables

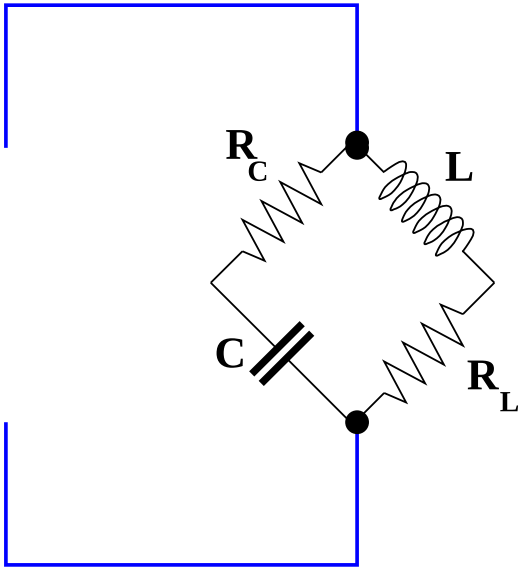
The *manifest variable assignment* is a map that assigns the manifest variables as a function of the terminal variables.

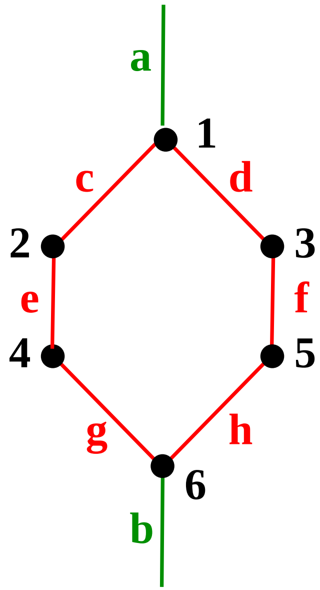
The terminal variables are henceforth considered as latent variables.

Behavioral equations

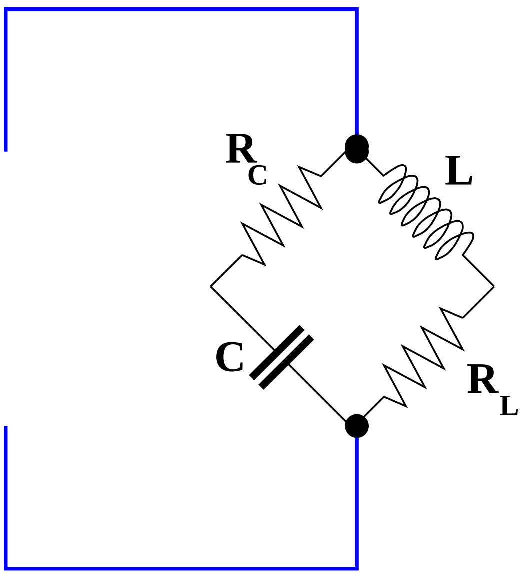
1. Module equations for each vertex
2. Interconnection constraints for each edge
3. Manifest variable assignment

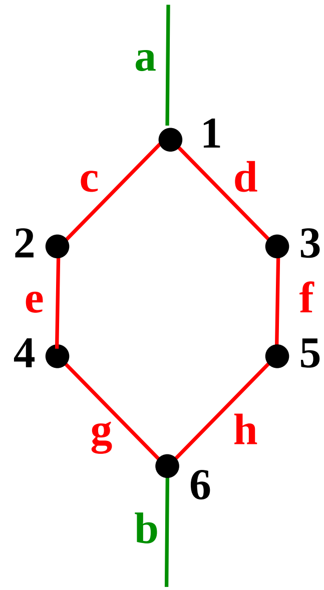
Example





Example





$$R_C \mapsto 2, R_L \mapsto 5, C \mapsto 4, L \mapsto 3, \text{connector}_1 \mapsto 1, \text{connector}_2 \mapsto 6,$$

$$1_{R_C} \mapsto c, 2_{R_C} \mapsto e, 1_{R_L} \mapsto f, 2_{R_L} \mapsto h, 1_C \mapsto e, 2_C \mapsto g, 1_L \mapsto d, 2_L \mapsto f,$$

$$1_{connector_1} \mapsto a, 2_{connector_1} \mapsto c, 3_{connector_1} \mapsto d,$$

$$1_{connector_2} \mapsto b, 2_{connector_2} \mapsto g, 3_{connector_2} \mapsto h.$$

Module equations

vertex 1 : $V_{1_{\text{connector}_1}} = V_{2_{\text{connector}_1}} = V_{3_{\text{connector}_1}},$

$I_{1_{\text{connector}_1}} + I_{2_{\text{connector}_1}} + I_{3_{\text{connector}_1}} = 0;$

vertex 2 : $V_{1_{R_C}} - V_{2_{R_C}} = R_C I_{1_{R_C}},\ I_{1_{R_C}} + I_{2_{R_C}} = 0;$

vertex 3 : $L\frac{d}{dt}I_{I_L} = V_{1_L} - V_{2_L},\ I_{1_L} + I_{2_L} = 0;$

vertex 4 : $C\frac{d}{dt}(V_{1_C} - V_{2_C}) = I_{1_C},\ I_{1_C} + I_{2_C} = 0;$

vertex 5 : $V_{1_{R_L}} - V_{2_{R_L}} = R_L I_{1_{R_L}},\ I_{1_{R_L}} + I_{2_{R_L}} = 0;$

vertex 6 : $V_{1_{\text{connector}_2}} = V_{2_{\text{connector}_2}} = V_{3_{\text{connector}_2}},$

$I_{1_{\text{connector}_2}} + I_{2_{\text{connector}_2}} + I_{3_{\text{connector}_2}} = 0.$

Interconnection equations

edge c : $V_{1_{R_C}} = V_{2_{\text{connector}_1}},\ I_{1_{R_C}} + I_{2_{\text{connector}_1}} = 0;$

edge d : $V_{1_L} = V_{3_{\text{connector}_1}},\ I_{1_L} + I_{3_{\text{connector}_1}} = 0;$

edge e : $V_{2_{R_C}} = V_{1_C},\ I_{2_{R_C}} + I_{1_C} = 0;$

edge f : $V_{2_L} = V_{1_{R_C}},\ I_{2_L} + I_{1_{R_C}} = 0;$

edge g : $V_{2_C} = V_{1_{\text{connector}_2}},\ I_{2_C} + I_{1_{\text{connector}_2}} = 0;$

edge h : $V_{2_{R_L}} = V_{2_{\text{connector}_2}},\ I_{2_{R_L}} + I_{2_{\text{connector}_2}} = 0.$

Manifest variable assignment

$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

Manifest variable assignment

$$V_{\text{external port}} = V_{1_{\text{connector}_1}} - V_{3_{\text{connector}_2}}$$

$$I_{\text{external port}} = I_{1_{\text{connector}_1}}$$

The module equations

+ interconnection constraints

+ manifest variable assignment

form the complete model for

$$V_{\text{external port}}, I_{\text{external port}}$$

Prevalence of latent variables. Elimination theory.

SUMMARY

- **Modeling by physical systems proceeds by tearing, zooming, and linking**

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- **Importance of latent variables and the elimination theorem**

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- **Modeling by physical systems proceeds by tearing, zooming, and linking**
- **Importance of latent variables and the elimination theorem**
- **Irrelevance of input/output thinking**

Details & copies of the lecture frames are available from/at

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Thank you

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