Remarks

on

RLC CIRCUITS

Jan C. Willems, K.U. Leuven

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THE REALIZATION PROBLEM

Given a set of building blocks,
and a way to interconnect these building blocks,
what behaviors can be obtained?

Example 1: State representation algorithms. Building blocks:
adders, amplifiers, forks, integrators
(as in analog computers)

$$\rightsquigarrow \quad \text{LTIDS} \quad \dot{\mathrm{x}} = A\mathrm{x} + B\mathrm{u}, \quad \mathrm{y} = C\mathrm{x} + D\mathrm{u}.$$

Example 2: Electrical circuit synthesis. Building blocks:
resistors, capacitors, inductors, connectors,
transformers, gyrators.

BUILDING BLOCKS

Module Types:

Resistors, Capacitors, Inductors, Transformers, Connectors.

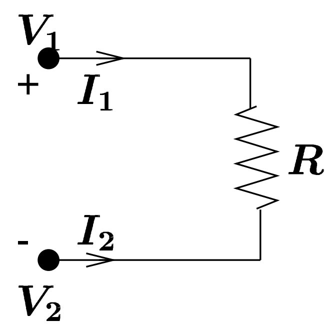
All terminals are of the same type: electrical,
and there are 2 variables associated with each terminal,

$$(V, I)$$

V **the *potential*,**
I **the *current* (counted > 0 when it flows into the module).**

$\rightsquigarrow$ **signal space of each terminal: $\mathbb{R}^2$.**

BUILDING BLOCKS



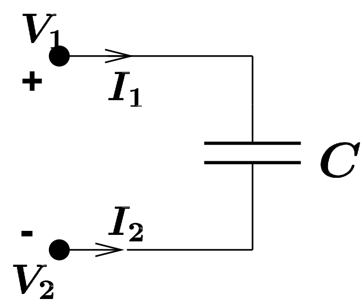
Resistor: **2-terminal module.**

Parameter: $R > 0$ **(resistance in ohms, say).**

Device laws:

$$V_1 - V_2 = R\,I_1\;; \quad I_1 + I_2 = 0.$$

BUILDING BLOCKS



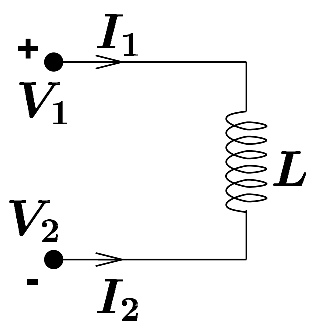
Capacitor: 2-terminal module.

Parameter: $C > 0$ (capacitance in farads, say).

Device laws:

$$C \frac{d}{dt}(V_1 - V_2) = I_1 \, ; \quad I_1 + I_2 = 0.$$

BUILDING BLOCKS



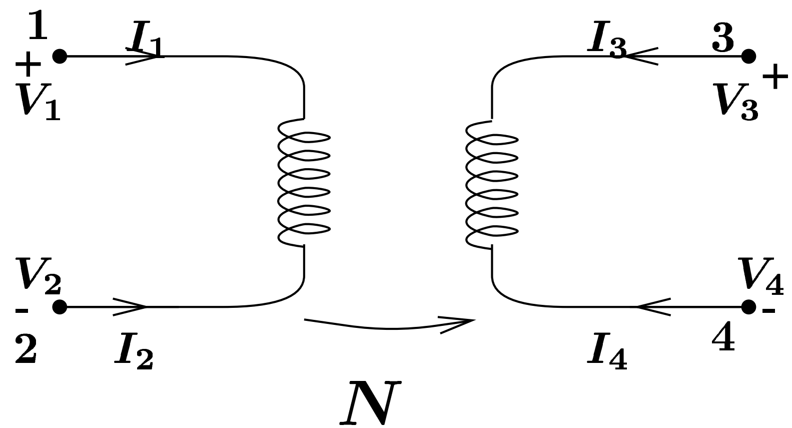
Inductor: 2-terminal module.

Parameter: $L > 0$ (inductance in henrys, say).

Device laws:

$$L\,\frac{d}{dt}I_1 = V_1 - V_2\,; \quad I_1 + I_2 = 0.$$

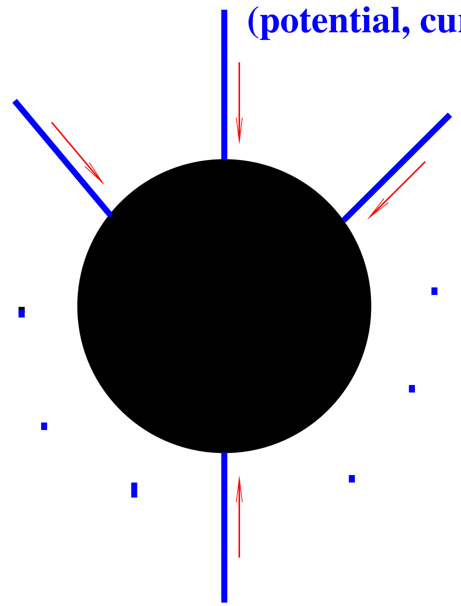
BUILDING BLOCKS



Transformer: 4-terminal module; terminals (1,2): primary;
terminals (3,4): secondary.
Parameter: $N \in \mathbb{R}$ (the turns ratio, $\in (0, \infty)$).
Device laws:

$$V_3 - V_4 = N(V_1 - V_2); I_1 = -NI_3;$$
$$I_1 + I_2 = 0; I_3 + I_4 = 0.$$

BUILDING BLOCKS



Connector: **many-terminal module.**

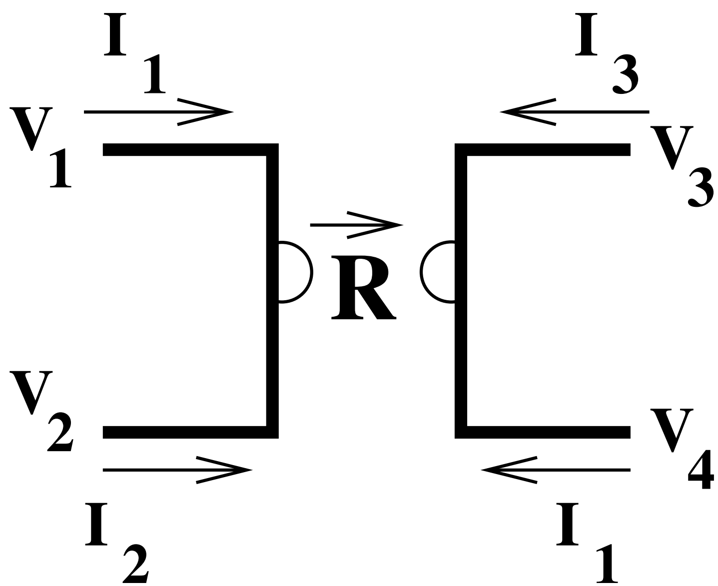
Parameter: $\mathtt{n}$ **(number of terminals, an integer).**

Device laws:

$$V_1 = V_2 = \cdots = V_{\mathrm{n}}\,; \quad I_1 + I_2 + \cdots + I_{\mathrm{n}} = 0.$$

BUILDING BLOCKS

In more advanced applications, we also meet the



Gyrator: 4-terminal module; (1,2): primary; (3,4): secondary.

Parameter: $R \in \mathbb{R}$ (gyrator resistance, in Ohms, say).

Device laws:

$$V_1 - V_2 = RI_3; V_3 - V_4 = -RI_1;$$

$$I_1 + I_2 = 0; I_3 + I_4 = 0.$$

INTERCONNECTION

Assume that terminal 1, with terminal variables V_1, I_1, is connected to terminal 2, with terminal variables V_2, I_2.

$\rightsquigarrow$ **Interconnection constraint:**

$$\mathcal{I}(V_1, I_1, V_2, I_2): \qquad V_1 = V_2, I_1 + I_2 = 0.$$

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Now interconnect terminals of a (finite) number of building blocks.

The result is called a(n **electrical) circuit**.

INTERCONNECTION

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$\rightsquigarrow$ Interconnection constraint:

$$I(V_1, I_1, V_2, I_2) : \qquad V_1 = V_2, I_1 + I_2 = 0.$$

Call the 'unconnected' terminals, the external terminals.

Number them: $(1, 2, \ldots, |E|)$.

Take as manifest variables of the circuit, the external terminal voltages and currents : $\Pi_{k \in |E|} \ (V_k, I_k)$.

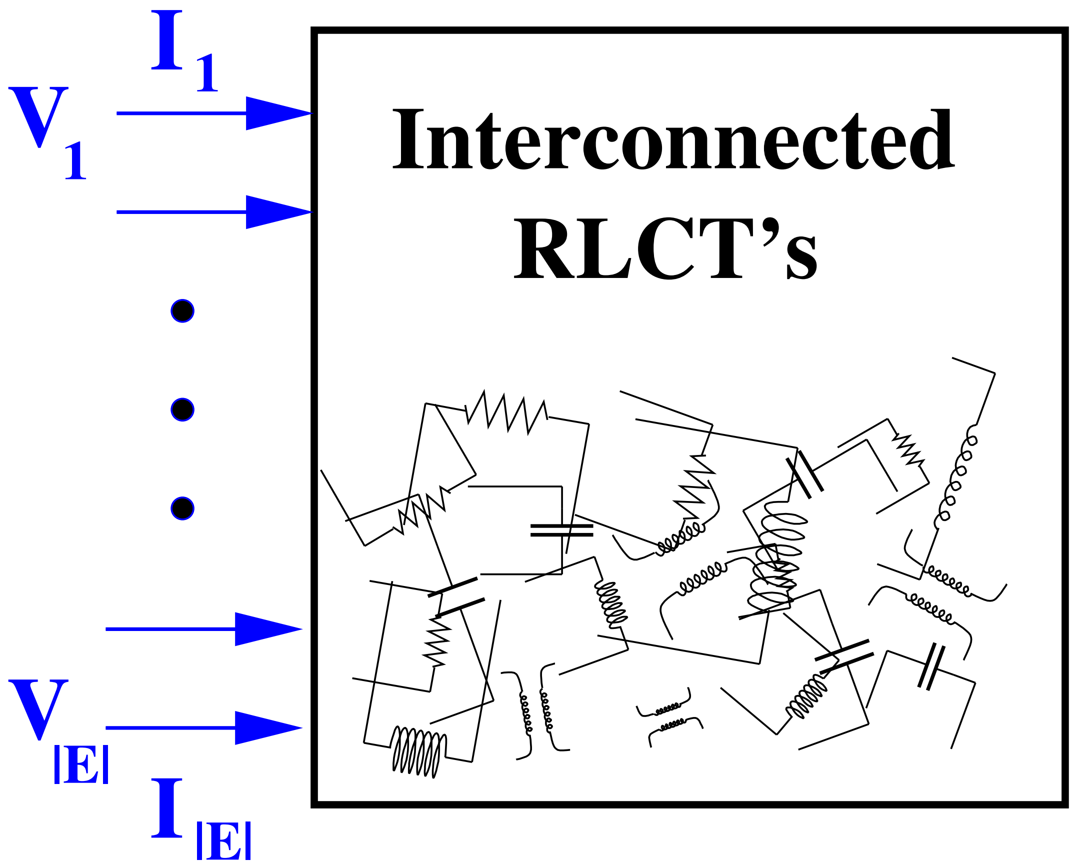
Denote $\Pi_{k \in |E|} \ (V_k, I_k)$ as $(V, I) \in \mathbb{R}^{2|E|}$.

By carrying out the interconnections, we end up with a system

$$(\mathbb{R}, \mathbb{R}^{2|E|}, \mathfrak{B}),$$

with external behavior: $\mathfrak{B} \subseteq (\mathbb{R}^{2|E|})^{\mathbb{R}}$.

INTERCONNECTION



CIRCUIT SYNTHESIS

The electrical circuit synthesis problem can be stated as follows:

***Realizability:* Which external behaviors can be obtained by interconnecting a finite number of R's, C's, L's, and T's? (or without T's, or with also G's?)**

CIRCUIT SYNTHESIS

The electrical circuit synthesis problem can be stated as follows:

***Realizability:* Which external behaviors can be obtained by interconnecting a finite number of R's, C's, L's, and T's? (or without T's, or with also G's?)**

***Synthesis:* If a behavior is realizable, give a *wiring diagram* (an architecture) that leads to the desired external behavior.**

This problem is of great importance (historical and otherwise) in electrical engineering. Important names:

Otto Brune	**R.M. Foster**	**W. Cauer**
E.A. Guillemin	**Sidney Darlington**	**A.D. Fialkow**
B.D.H. Tellegen	**Dante Youla**	**Vitold Belevitch**
etc., etc.		

CIRCUIT SYNTHESIS

We list seven necessary conditions!

We now discuss these conditions, aiming at demonstrating

- **the relevance of passivity and positive realness**
- **the ease of analysis provided by the behavioral approach**

CIRCUIT SYNTHESIS

We list seven necessary conditions!

1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$

i.e., $\Sigma = (\mathbb{R}, \mathbb{R}^{2|E|}, \mathfrak{B})$ **is a LTIDS. There are** ∞ **ways of stating what this means.**

For example, there exists a polynomial matrix $R^{\bullet \times 2|E|} \in \mathbb{R}[\xi]$ **such that** $\mathfrak{B}$ **consists of the solutions of**

$$R(\frac{d}{dt}) \begin{bmatrix} V \\ I \end{bmatrix} = 0.$$

Proof: Elimination th'm.

CIRCUIT SYNTHESIS

We list seven necessary conditions!

1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$
2. **KVL**

$$(V, I) \in \mathfrak{B} \text{ and } \alpha \in \mathfrak{C}^{\infty}(\mathbb{R}, \mathbb{R}) \Rightarrow (V + \alpha e, I) \in \mathfrak{B}$$

with

$$e = \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}$$

Proof: **Verify for each of the modules, and for the int. constraint.**

CIRCUIT SYNTHESIS

We list seven necessary conditions!

1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$
2. **KVL**
3. **KCL**

$$(V, I) \in \mathfrak{B} \Rightarrow e^\top I = 0$$

with

$$e = \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}$$

Proof: **Verify for each of the modules, and for the int. constraint.**

CIRCUIT SYNTHESIS

We list seven necessary conditions!

1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$
2. **KVL**
3. **KCL**
4. **The input cardinality,** $\mathtt{m}(\mathfrak{B}) = |E|$

In other words, there exist a partition of (V, I) in $|E|$ inputs and $|E|$ outputs, with, if you insist, a proper transfer function.

Consider this together with the next property.

CIRCUIT SYNTHESIS

We list seven necessary conditions!

1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$
2. KVL
3. KCL
4. The input cardinality, $\mathtt{m}(\mathfrak{B}) = |E|$
5. Hybridicity

There exists an I/O repr. for which the input and output var.

$$(u_1, u_2, \ldots, u_{|E|}), \ (y_1, y_2, \cdots, y_{|E|})$$

pair as follows:

$$\{u_{\mathrm{k}}, y_{\mathrm{k}}\} = \{V_{\mathrm{k}}, I_{\mathrm{k}}\}$$

In other words, each terminal is either

current controlled or voltage controlled.

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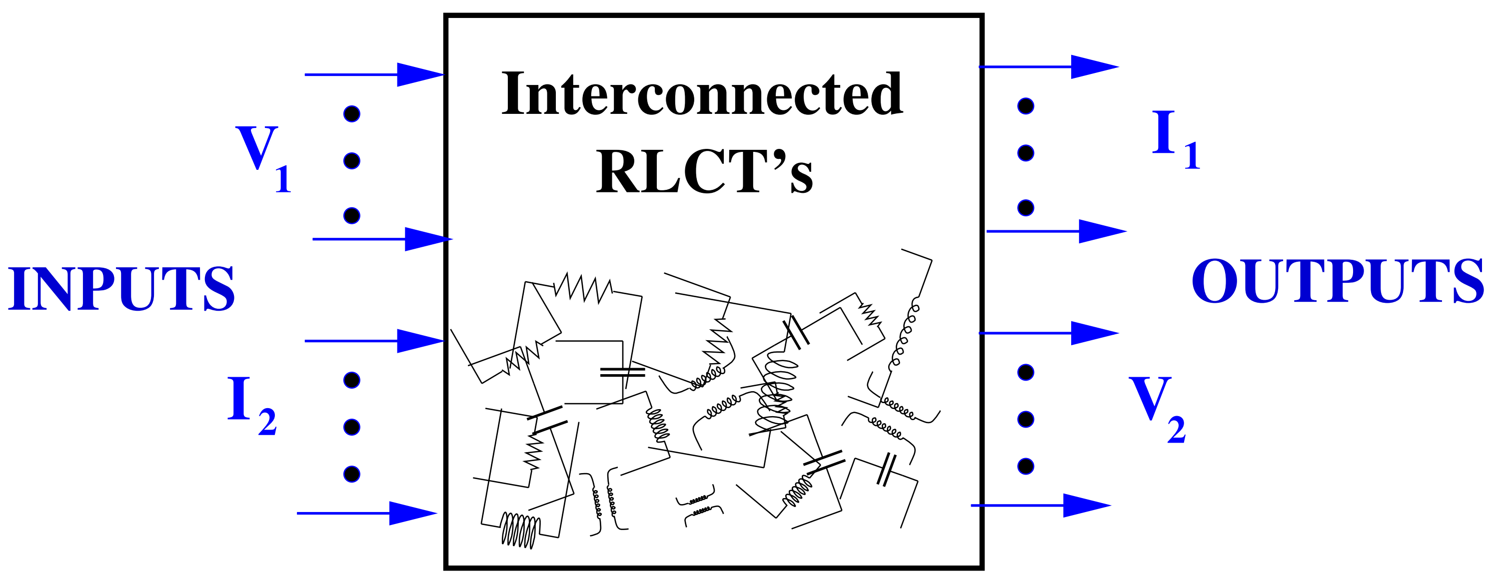

CIRCUIT SYNTHESIS

We list seven necessary conditions!

1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$
2. **KVL**
3. **KCL**
4. **The input cardinality,** $\mathtt{m}(\mathfrak{B}) = |E|$
5. **Hybridicity**
6. **Passivity.** From hybridicity, $\mathfrak{B}$ admits a representation as

$$\overset{\bullet}{x} = Ax + Bu, \;\; y = Cx + Du$$

This system is dissipative w.r.t. the supply rate $u^\top y = V^\top I$**,**
and with a quadratic positive definite storage f'n

$$V(x) = x^\top K x, K = K^\top > 0.$$

This states that the net electrical energy goes into the circuit.

CIRCUIT SYNTHESIS

We list seven necessary conditions!

1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$
2. **KVL**
3. **KCL**
4. **The input cardinality,** $\mathtt{m}(\mathfrak{B}) = |E|$
5. **Hybridicity**
6. **Passivity.** **It is easiest to prove properties 4, 5, and 6 together.**

6: a circuit is an interconnection of passive elements, with neutral interconnection laws.

4 and 5: holds for passive circuits, prove it by considering one interconnection at the time.

CIRCUIT SYNTHESIS

We list seven necessary conditions!

1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$
2. KVL
3. KCL
4. The input cardinality, $\mathtt{m}(\mathfrak{B}) = |E|$
5. Hybridicity
6. Passivity.
7. Reciprocity. The transfer f'n G is signature symmetric, i.e.

$$\Sigma G = G^\top \Sigma.$$

Σ is the signature matrix $\Sigma = \mathrm{diag}(s_1, s_2, \ldots, s_{|E|})$,
with $s_\mathrm{k} = +1$ if terminal k is voltage controlled,
and $s_\mathrm{k} = -1$ if terminal k is current controlled.

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This curious properties may be translated as:

The influence of terminal $\mathtt{k}'$ on terminal $\mathtt{k}''$ is equal to the influence of terminal $\mathtt{k}''$ on terminal $\mathtt{k}'$.

CIRCUIT SYNTHESIS

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1. $\mathfrak{B} \in \mathfrak{L}^{2|E|}$
2. **KVL**
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4. **The input cardinality,** $\mathtt{m}(\mathfrak{B}) = |E|$
5. **Hybridicity**
6. **Passivity.**
7. **Reciprocity.**

Proof: **Show that each of the modules satisfy property (7). Show that this property remain valid after interconnection, i.e. proceed again one interconnection at the time.**

CIRCUIT SYNTHESIS

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4. The input cardinality, $\mathtt{m}(\mathfrak{B}) = |E|$
5. Hybridicity
6. Passivity.
7. Reciprocity.

If $\mathfrak{B}$ is controllable then these conditions are also sufficient for realizability. However, in order to obtain a 'clean' statement, it is convenient to eliminate $I_{|E|} = -I_1 - I_2 - \cdots - I_{|E|-1}$, and look at the behavior of $(V_1 - V_{|E|}, V_2 - V_{|E|}, \ldots, V_{|E|-1} - V_{|E|}, I_1, I_2, \ldots, I_{|E|-1})$.

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5. **Hybridicity**
6. **Passivity.**
7. **Reciprocity.**

The transfer function $G \in \mathbb{R}^{(|E|-1)\times(|E|-1)}$ ***is realizable using RLCT's if and only if it is signature symmetric and positive real.***

CIRCUIT SYNTHESIS

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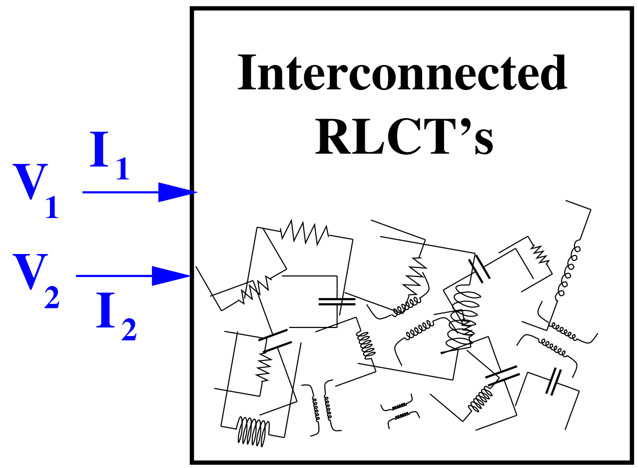
The transfer function $G \in \mathbb{R}^{(|E|-1)\times(|E|-1)}$ ***is realizable using RLCTG's if and only if it is positive real.***

SYNTHESIS of DRIVING POINT IMPEDANCES

Consider a 2-terminal circuit



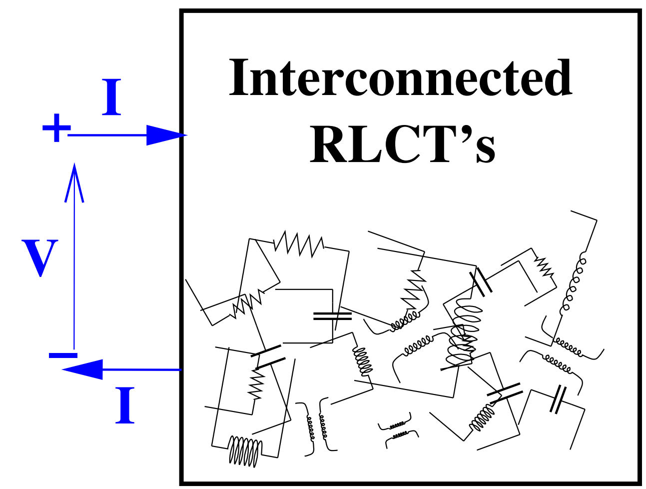
KCL $\Rightarrow$ $I_1 + I_2 = 0.$ **Set** $\boldsymbol{I := I_1 = -I_2}$.

KVL $\Rightarrow$ **the beh. eq'ns involve only** $V_1 - V_2$. **Set** $\boldsymbol{V := V_1 - V_2}$.

The behavior of (V, I) **is called the port description.**

SYNTHESIS of DRIVING POINT IMPEDANCES

Port description:



Z, the transfer f'n $I \mapsto V$ is called the **driving point impedance**.
Note that Z need not be proper.

Which driving point impedances are realizable?

SYNTHESIS of DRIVING POINT IMPEDANCES

Which driving point impedances are realizable?

$Z \in \mathbb{R}(\xi)$ is the driving point impedance
of an electrical circuit that consists of an interconnection
of a finite number of
positive R's, positive L's, positive C's, and transformers
if and only if Z is positive real.

SYNTHESIS of DRIVING POINT IMPEDANCES

Which driving point impedances are realizable?

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of an electrical circuit that consists of an interconnection
of a finite number of
positive R's, positive L's, positive C's, and transformers
if and only if Z is positive real.

This result led to the introduction of positive real functions.
First proven by Otto Brune in his M.I.T. Ph.D. dissertation (see O. Brune, *Synthesis of a finite two-terminal network whose driving point impedance is a prescribed function of frequency,* Journal of Mathematics and Physics, volume 10, pages 191-236, 1931).

SYNTHESIS of DRIVING POINT IMPEDANCES

Which driving point impedances are realizable?

$Z \in \mathbb{R}(\xi)$ is the driving point impedance of an electrical circuit that consists of an interconnection of a finite number of positive R's, positive L's, positive C's, and transformers if and only if Z is positive real.

Are transformers needed?

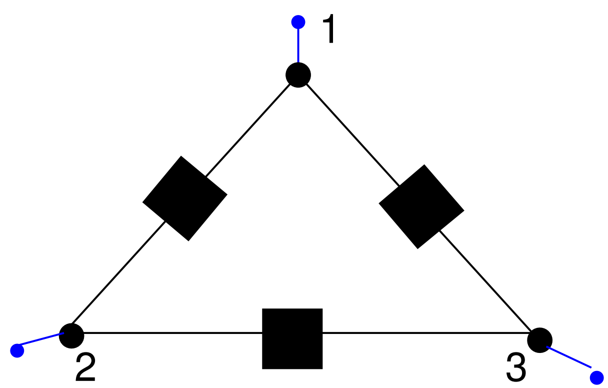
In 1949, Bott and Duffin proved 'no' in a one-page (!) paper (see R. Bott and R.J. Duffin, *Impedance synthesis without transformers,* Journal of Applied Physics, vol. 20, page 816, 1949).
However, their synthesis has common factors, non-controllability!

REMARK

TERMINALS versus PORTS

Note that we have used throughout the terminal description of circuits. It is simply more appropriate and more general (even when using only 'port' devices).

Example:



However, port descriptions are more parsimonious in the choice of variables (it halves their number).

RECAP

- **Realizability theory: an important engineering oriented problem area.**
- **The analysis and synthesis of RLCT circuits is an important application of passive systems.**
- **7 necessary conditions for realizability by passive R,L,C,T's:**
  differential system, KVL, KCL, input cardinality, hybridicity, passivity, and reciprocity.
- **In the controllable case these conditions are also sufficient.**
- **It is the circuit synthesis problem that led to positive realness.**