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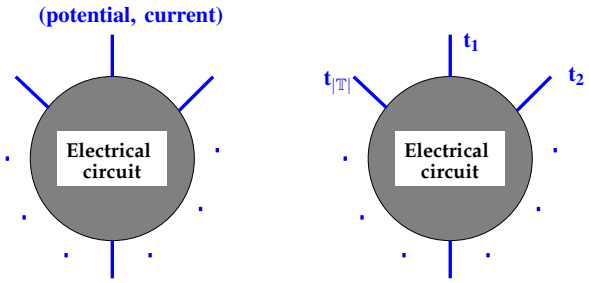
The Behavior of Linear Time Invariant RLC Circuits

Erik I. Verriest and Jan C. Willems

Abstract— **It is shown that just as we did for a purely resistive network [10], that circuit analysis is very simple if the elements are described not by potentials across and currents through the elements, but rather by the potentials at the nodes and the external currents into the nodes. For simple R, C or L components this gives a description with a 2×2 matrix, which is more complex than the scalar constitutive laws governing the potential across and current through. However this description has an advantage in performing the analysis of more complicated circuits. These are built up from simple operations like joining two nodes, splicing at nodes, and minimalization.**

I. Introduction: Terminal behavior

We view an electrical circuit as a device that interacts with its environment through a finite number of wires (henceforth called *terminals* and denoted by $t_1, t_2, \ldots, t_{|\mathbb{T}|}$), as illustrated in the figure below. Associated with each terminal, there is a



potential and a *current* (by convention counted positive when it runs into the circuit). Even though only potential differences are physically measurable, we consider the terminal potentials and the currents as the essential quantities which describe how a circuit interacts with its surroundings. The physical meaning of the potentials is the potential differences with an arbitrary common point, that can vary over time, and be external or internal to the circuit. KVL implies that one may use these potentials instead of the voltages across the terminals [9].

Assuming that potentials and currents are expressed in some units (say, volts and amps), we obtained in [10] that the instantaneous interaction of the circuit with its surroundings is specified by a vector $(P,I) \in \mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|}$. In this paper we extend our results from memoryless circuits to RLC-circuits. Hence the instantaneous behavior no longer suffices to describe the circuit. The set of functions $(P,I) \in (\mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|})^{\mathbb{R}}$ that are compatible with the internal structure of the circuit and component values forms a subset $\mathscr{B} \subseteq (\mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|})^{\mathbb{R}}$, called the *terminal behavior* of the circuit. $(P,I) \in \mathscr{B}$ means that the circuit allows the vector functions (P,I) of terminal variables, while $(P,I) \notin \mathscr{B}$ means that the circuit forbids the vector (P,I) of terminal variable functions [7], [8]. In this paper, we study which subsets $\mathscr{B} \subseteq (\mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|})^{\mathbb{R}}$ can occur as the terminal potential/current behavior of an interconnection of a finite set of linear nonnegative resistors, inductors and capacitors. The paper is organized as follows: In Section II, the purely resistive network is revisited, and the full characterization we obtained for the behavioral description are stated. The main goal is to extend these to time-invariant RLC circuits. One approach, starting from purely resistive, inductive and capacitive circuits is sketched in Section III. In order to shed some light on the properties of this operator, an alternative component-wise building up of the circuit from its constituent elements is given in section IV. It leads to a set of necessary conditions for the matrix representing the manifest potential/current at the external terminals.

Erik I. Verriest is with the Department of ECE, Georgia Institute of Technology, Atlanta, GA 30332-0250, USA. He was on sabbatical with SCD, ESAT, KULeuven, Leuven, B-2001, Belgium while part of this work was prepared. Erik.Verriest@ece.gatech.edu

Jan C. Willems is with the Department of Electrical Engineering, KULeuven, Leuven, B-2001, Belgium. Jan.Willems@esat.kuleuven.be

II. Behavioral equations of a resistive circuit

There are a number of ways to arrive at equations for the terminal behavior of a linear resistive circuit. The classical way of introducing as auxiliary variables the vertex potentials and the edge currents is convenient and general. Label the vertices as $v_1, v_2, \ldots, v_{|\mathbb{V}|}$, the edges as $e_1, e_2, \ldots, e_{|\mathbb{E}|}$ (assuming there are no self-loops), and the leaves (which correspond to the external terminals) as $t_1, t_2, \ldots, t_{|\mathbb{T}|}$. Assign a direction to each edge. Now introduce the *edge incidence matrix* $\mathbb{I}_{\mathbb{E}} \in \{1,-1,0\}^{|\mathbb{V}|\times|\mathbb{E}|}$ and the *leaf incidence matrix* $\mathbb{I}_{\mathbb{T}} \in \{1,0\}^{|\mathbb{V}|\times|\mathbb{T}|}$ by

$$(\mathbb{I}_{\mathbb{E}})_{i,j} = \begin{cases} 1 & \text{if } e_i \text{ is incident to and directed towards } v_j, \\ -1 & \text{if } e_i \text{ is incident to and directed away from } v_i, \\ 0 & \text{if } e_i \text{ is not incident to } v_j, \end{cases}$$

$$(\mathbb{I}_{\mathbb{L}})_{i,j} = \begin{cases} 1 & \text{if } \ell_i \text{ is incident to } v_j \\ 0 & \text{if } \ell_i \text{ is not incident to } v_j. \end{cases}$$

Introduce the vector of vertex potentials $P_{\mathbb{V}}$, of edge currents $I_{\mathbb{E}}$, of leaf (external terminal) potentials P, and of leaf (external terminal) currents I

$$P_{\mathbb{V}} = \begin{bmatrix} P_{v_1} \\ P_{v_2} \\ \vdots \\ P_{v_{|\mathbb{V}|}} \end{bmatrix}, \quad I_{\mathbb{E}} = \begin{bmatrix} I_{e_1} \\ I_{e_2} \\ \vdots \\ I_{e_{|\mathbb{E}|}} \end{bmatrix}, \quad P = \begin{bmatrix} P_{t_1} \\ P_{t_2} \\ \vdots \\ P_{t_{|\mathbb{T}|}} \end{bmatrix}, \quad I = \begin{bmatrix} I_{t_1} \\ I_{t_2} \\ \vdots \\ I_{t_{|\mathbb{T}|}} \end{bmatrix}. \quad (1)$$

Introduce also the *edge resistance matrix* $R \in [0,\infty)^{|\mathbb{E}|\times|\mathbb{E}|}$, the diagonal matrix with elements $\rho(e_1),\rho(e_2),\ldots,\rho(e_{|\mathbb{E}|})$ on the diagonal.

The behavioral equations of the circuit can be written compactly as

$$\mathbb{I}_{\mathbb{E}} P_{\mathbb{V}} + R I_{\mathbb{E}} = 0, \quad \mathbb{I}_{\mathbb{E}}^{\top} I_{\mathbb{E}} + \mathbb{I}_{\mathbb{L}}^{\top} I = 0, \quad \mathbb{I}_L P_{\mathbb{V}} = P. \tag{2}$$

The first of these equations expresses that the potential drop across each vertex is equal to the resistance times the current. The second equation expresses that the algebraic sum of the currents that flow into each vertex is zero (recall that we have chosen the terminal currents to be positive when they run into the circuit). The third equation expresses that the potential of an external terminal is equal to the potential of the vertex to which the corresponding leaf is incident.

Equations (2) specify the terminal behavior of the resistive circuit. As is common when modeling interconnected systems, these equations contain auxiliary ('latent') variables (the vertex potentials and edge currents $P_{\mathbb{V}}, I_{\mathbb{E}}$) in addition to the ('manifest') variables (the terminal potentials and currents P, I) which the model aims at. The terminal potential/current behavior is given by

$$\mathscr{B} = \{(P,I) \in \mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|} \mid \exists\ (P_{\mathbb{V}}, I_{\mathbb{E}}) \in \mathbb{R}^{|\mathbb{V}|} \times \mathbb{R}^{|\mathbb{E}|} \text{s.t.} (2)\}.$$

Since these equations are linear, the latent variables variables can be completely eliminated, resulting in a set of linear relations: $L_V P + L_I I = 0$, for the manifest variables. In total we have $|\mathbb{V}| + |\mathbb{E}|$ latent and $2|\mathbb{T}|$ manifest variables, related by the $|\mathbb{V}| + |\mathbb{E}| + |\mathbb{T}|$ equations (2). were derived in [10]. It was shown that $|\mathbb{T}|$ (= $(|\mathbb{V}| + |\mathbb{E}| + 2|\mathbb{T}|) - (|\mathbb{V}| + |\mathbb{E}| + |\mathbb{T}|)$) equations relate (V,I). A somewhat different approach, via the weighted Laplacian matrix of a graph is presented in [5]. We restate first the main result in [10].

Theorem 1: In a suitable ordering of the terminals of a linear resistive circuit, the equations governing the terminal behavior take the following specific form. There exist positive integers $N_1, N_2, \ldots, N_k$ with $N_1 + N_2 + \cdots + N_k = |\mathbb{T}|$ so that the behavioral equations take the form

$$\begin{aligned}
P_{t_1} = P_{t_2} = \cdots = P_{t_{N_1}} &=: \tilde{P}_1 \\
P_{t_{N_1+1}} = P_{t_{N_1+2}} = \cdots = P_{t_{N_1+N_2}} &=: \tilde{P}_2 \\
\vdots \qquad\qquad\qquad\qquad &\vdots \\
P_{t_{|\mathbb{T}|-N_k+1}} = P_{t_{|\mathbb{T}|-N_k+2}} = \cdots = P_{|\mathbb{T}|} &=: \tilde{P}_k
\end{aligned} \tag{3}$$

$$\begin{aligned}
\tilde{I}_1 &:= I_{t_1} + I_{t_2} + \cdots + I_{t_{N_1}} \\
\tilde{I}_2 &:= I_{t_{N_1+1}} + I_{t_{N_1+2}} + \cdots + I_{t_{N_1+N_2}} \\
&\vdots \qquad\qquad\qquad\qquad \vdots \\
\tilde{I}_k &:= I_{t_{|\mathbb{T}|-N_k+1}} + I_{t_{|\mathbb{T}|-N_k+2}} + \cdots + I_{|\mathbb{T}|}
\end{aligned} \tag{4}$$

combined with

$$\begin{bmatrix} \tilde{I}_1 \\ \tilde{I}_2 \\ \vdots \\ \tilde{I}_k \end{bmatrix} = G \begin{bmatrix} \tilde{P}_1 \\ \tilde{P}_2 \\ \vdots \\ \tilde{P}_k \end{bmatrix}, \tag{5}$$

with $G \in \mathbb{R}^{k\times k}$ a square matrix satisfying

(i) $G_{i,i} \geq 0 \quad \text{for } i = 1,2,\ldots,k,$
(ii) $G_{i,j} = G_{j,i} \leq 0 \quad \text{for } i,j = 1,2,\ldots,k, i \neq j$
(iii) $\sum_{i=1}^{k} G_{i,j} = \sum_{j=1}^{k} G_{i,j} = 0 \quad \text{for } i,j = 1,2,\ldots,k.$

Square matrices satisfying (i), (ii), and (iii) are called *symmetric hyperdominant with zero excess*.

Conversely, for a set of equations having the structure of equations (4, 5), with $G \in \mathbb{R}^{k\times k}$ symmetric hyperdominant with zero excess, there exists a linear resistive circuit with these terminal potential/current behavioral equations.

III. General admittance description

The port behavioral description of a capacitor is similar to that of the resistor

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} C & -C \\ -C & C \end{bmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} P_1 \\ P_2 \end{bmatrix}. \tag{6}$$

Obviously, this is equivalent to the set $I_1 = C\frac{\mathrm{d}}{\mathrm{d}t}(P_1 - P_2)$. and $I_1 + I_2 = 0$. But unlike the R and the C, the inductor behavioral equations $(I_1 + I_2 = 0, P_1 - P_2 = L\frac{\mathrm{d}}{\mathrm{d}t} I_1$ are *not* unimodularly equivalent to the symmetrical form

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \Gamma & -\Gamma \\ -\Gamma & \Gamma \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \end{bmatrix}, \tag{7}$$

as the latter only implies constancy of the sum $I_1 + I_2$.

Just as in the specification for the purely resistive network, the topology or architecture of the RLC circuit is a digraph with leaves without self loops. The edges correspond to the circuit elements. Introduce three $|\mathbb{E}| \times |\mathbb{E}|$ diagonal matrices, $\mathscr{R}$, $\mathscr{L}$ and $\mathscr{C}$ defined respectively as follows: $\mathscr{R}_{ii} = R(e_i)$ if there is a resistor with resistance $R(e_i)$ in edge e_i, and 0 else. Likewise $\mathscr{L}_{ii} = L_(e_i)$ if there is an inductor of value $L(e_i)$ and 0 else, and $\mathscr{C}_{ii} = C(e_i)$ if there is an capacitor of value $C(e_i)$ in the edge e_i, and 0 else. The proper extension of (2) is then the set of equations (see [9])

$$\begin{aligned}
\mathscr{Y}\left(\frac{\mathrm{d}}{\mathrm{d}t}\right) \mathbb{I}_{\mathbb{E}} P_{\mathbb{V}} + \mathscr{Z}\left(\frac{\mathrm{d}}{\mathrm{d}t}\right) I_{\mathbb{E}} = 0, \\
\mathbb{I}_{\mathbb{E}}^{\top} I_{\mathbb{E}} + \mathbb{I}_{\mathbb{L}}^{\top} I = 0, \quad \mathbb{I}_L P_{\mathbb{V}} = P,
\end{aligned} \tag{8}$$

where the polynomial matrices $\mathscr{Z}(\xi)$ and $\mathscr{Y}(\xi)$ are diagonal and $\mathscr{Z}_{ii}(\xi) = (\mathscr{R} + \mathscr{L}\xi)_{ii}$ if that element is nonzero,and 0 else. Likewise, $\mathscr{Y}_{ii}(\xi) = (\mathscr{C}\xi)_{ii}$ if that element is nonzero,and 0 else. These equations define the current/potential behavior of the circuit as

$$\mathscr{B} = \{(I,P) \in \mathbb{R}^{|\mathbb{T}|\times|\mathbb{T}|} \mid \exists\ (I_{\mathbb{E}}, P_{\mathbb{V}}) \in \mathbb{R}^{|\mathbb{E}|} \times \mathbb{R}^{|\mathbb{V}|} \text{s.t.} (8)\}.$$

This description has the latent variables $I_{\mathbb{E}}$ and $P_{\mathbb{V}}$ in it. Eliminating these is not an easy matter. What makes it difficult is the controllability issue. If one does not worry about controllability, one may proceed with the transfer functions (see below). The issue about the interpretaion of differential equations involving rational functions emerges [11]. This approach results in an extension of the resistive network result, i.e., some symmetric hyperdominant with zero excess structure. In [9] this is shown in terms of (real) exponential solutions.

Can one exploit more structure? Similar to (5), in the compact form $I_R = GP_R$, we can obtain an exhaustive description for a purely capacitive network

$$I_C = C\frac{d}{dt}P_C. \tag{9}$$

The matrix C has diagonal elements C_{ii}=sum of capacities of the capacitors connected to leaf i, and C_{ij} = negative of the capacity between leaf i and j. Since the behavioral equations for an inductor imply a symmetric description (7), a *partial* behavioral description of a purely inductive network is, in a compact form,

$$\frac{d}{dt}I_L = \Gamma P_L.$$

The matrix Γ has diagonal elements Γ_{ii}=sum of inverses of the inductances of the inductors connected to leaf i, and Γ_{ij} = negative of the inverse inductance, L_{ij}^{-1} between leaf i and j. The remaining equations (KCL for inductors) further constrain the behavior.

Note that C and Γ are matrices of the same form as G in the purely resistive network we described earlier. Consequently they possess the symmetric, hyperdominant, zero-excess structure.

As an alternative approach, one can construct a circuit by joining the resistive, inductive and capacitive parts and then eliminate the nodes that are not necessary in the behavioral description (i.e., the internal nodes).

To this effect, single out the leaves in the resistive circuit that will remain (external) after connection, and partition the other in leaves that connect to either terminals from the inductive or the capacitive circuit. Likewise identify the nodes connected to leaves and the nodes to be eliminated in the inductive and capacitive circuit. The heavy lines in Figure 1 denote collections of terminals. However as ultimately connections will be made, it is understood that $\dim I_{LR} = \dim I_{RL}$, and similarly for the other doubly indexed current and potential vectors.

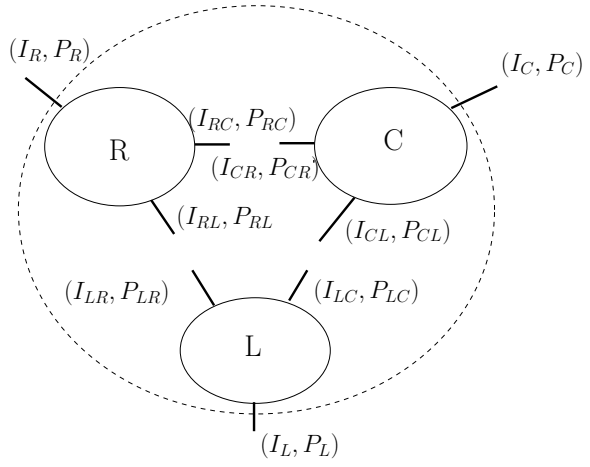


Fig. 1. Joining R L and C

Thus

$$\begin{bmatrix} I_R \\ I_{RC} \\ I_{RL} \end{bmatrix} = \begin{bmatrix} \quad \\ G \\ \quad \end{bmatrix} \begin{bmatrix} P_R \\ P_{RC} \\ P_{RL} \end{bmatrix}$$

with similar forms for the capacitive and inductive circuits. After elimination, the RCL network enclosed by the dotted line in Figure 1 results. However,as before issues of controllability (actually lack of it) may occur, whenever Schur complements are taken. Controllability is equivalent to right coprimeness of certain polynomial matrices in the equations. Note that each of the matrices G, C and Γ is symmetric, hyperdominant with zero excess, but perhaps reducible, as shown in the example of Figure 2: The given RC circuit is decomposed first into a purely resistive and a purely capacitive circuit. For this we double up some of the terminals: Terminal 5 in the original RC circuit has a copy, 5', in the resistive and a copy, 5", in the capacitive circuit. Likewise terminals 2, 3 and 4, but not 1 are doubled. Consequently we introduce $I_R = I_1$, and $I_{RC} = [I_2, I_3, I_4, I_5]^T$, while $I_{CR} = [I'_2, I'_3, I'_4, I'_5]^T$, etc. Note that there are no I_C components, because no terminals connect to only a capacitor. Terminals of the R- and C-circuits with like numbers are connected (and if this vertex is not a terminal, eliminated). Combining the descriptions we get (see figure 1)

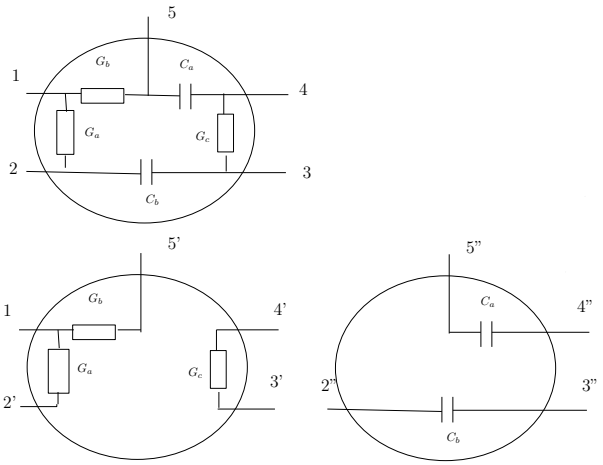


Fig. 2. Partial G and C circuits

$$\left[\begin{array}{c|c|c} I & & \\ \hline & I & \\ \hline & & \mathbf{D} \end{array}\right] \left[\begin{array}{c} I_R \\ I_{RC} \\ I_{RL} \\ \hline I_{CR} \\ I_C \\ I_{CL} \\ \hline I_{LR} \\ I_{LC} \\ I_L \end{array}\right] =$$

$$= \left[\begin{array}{c|c|c} G & & \\ \hline & C\mathbf{D} & \\ \hline & & \Gamma \end{array}\right] \left[\begin{array}{c} P_R \\ P_{RC} \\ VP_{RL} \\ \hline P_{CR} \\ P_C \\ P_{CL} \\ \hline P_{LR} \\ P_{LC} \\ P_L \end{array}\right],$$

together with the current constraints on the inductive subnetwork. Alternatively, we can do things 'right' from the beginning and use the behavioral equations $I_i + I_j = 0, I_i = \Gamma_{ij}\frac{\mathrm{d}}{\mathrm{d}t}(P_i - P_j)$ for each inductive component, and use the resulting nonsymmetric behaviorial description for the inductive part. Letting $I'_{\mathbb{T}} = [I'_R, I'_C, I'_L]$ and $P'_{\mathbb{T}} = [P'_R, P'_C, P'_L]$ elimination results in the matrix fraction description [2]

$$X(\mathbf{D}) \left[\begin{array}{c} I_{\mathbb{T}} \\ I_{in} \end{array}\right] = Y(\mathbf{D}) \left[\begin{array}{c} P_{\mathbb{T}} \\ P_{in} \end{array}\right]$$

describing the terminal behavior $\mathscr{B}$ and thus equivalent to (8). It is possible to eliminate the internal variable I_{in} and P_{in} and obtain a polynomial matrix description $F\left(\frac{\mathrm{d}}{\mathrm{d}t}\right) \left[\begin{array}{c} I_{\mathbb{T}} \\ P_{\mathbb{T}} \end{array}\right]$ [9].

IV. Building a circuit from its components

This is done in two steps. First, to allow for parallel combinations of distinct elements, we need to consider graphs, which are permitted to have several edges connected to the same two vertices. The first step then reduces the graph description to a simple graph (no parallel edges or self-loops), by reducing the number the edges between vertices to at most one. This is performed by induction, one edge at a time. The second step assumes that one leaf is incident to every vertex. Then take away one leaf, by letting its current be zero and eliminating the corresponding potential. The induction in both steps is shown in the representation of the behavioral equations.

A. Graph reduction

Let vertices v_i and v_j have k edges between them, labeled $e_1, \ldots, e_k$. We zoom in onto this subcircuit by disconnecting all edges connecting v_i to all vertices except v_j and likewise for the edges incident to v_j but not to v_i. This leaves just the parallel edges connecting v_i and v_j. Now disconnect $k-1$ edges from v_j and introduce $k-1$ new vertices, which together with the original v_j are labelled $v_{j_1}, \ldots, v_{j_k}$. This gives a star shaped graph (center at v_i), the corresponding circuit has the behavioral form, given in terms of the currents and potentials (I_i, P_i) and $(I_j = [I_{j_1}, \ldots, I_{j_k}]^T, P_j = [P_{j_1}, \ldots, P_{j_k}]^T)$

$$\left[\begin{array}{c} I_i \\ I_j \end{array}\right] = \left[\begin{array}{cc} \sum_{\ell=1}^k Y_{j\ell} & -Y_j^T \\ -Y_j & \mathrm{diag}\, Y_j \end{array}\right] \left[\begin{array}{c} P_i \\ P_j \end{array}\right]$$

where $Y_j^T = [Y_{j1} \cdots Y_{jk}]$ and $\mathrm{diag}\, Y_j$ is the diagonal matrix with $Y_{j\ell}$ in the ℓ-th position. The $Y_{j\ell}$ belong to $\mathbb{R}_+ \cap \mathbb{R}_+\xi \cap \mathbb{R}_+\xi^{-1}$. Consequently, the above matrix is symmetric and its row and column sums add to one. Moreover, since the admittances only involve elementary components, is only has terms in $\xi, 1$ and ξ^{-1}. Hence each of these three coefficient matrices is symmetric, hyperdominant with zero excess. Link now the j-vertices one at a time, by setting the corresponding potentials equal: $v_{j,k-1} = v_{jk}$, replacing the $I_{j,k-1}$-row by $I^{(1)}_{j,k-1} = I_{j,k-1} + I_{jk}$, and finally deleting the last row (corresponding to I_{jk}). This gives a $k-1 \times k-1$ matrix of the same form with as $(1,k-1)$- and $(k-1,1)$-entry $-y_{j,k-1} - y_{j,k}$, and last entry on the diagonal $y_{j,k-1} + y_{j,k}$. This new matrix is again the sum of three symmetric hyperdominant matrices with zero excess, respectively multiplied by ξ, 1, and ξ^{-1}. Now keep iterating until a 2×2 matrix results for the edge e_{ij}. Since at each step the structure is preserved, the graph with vertices $\{v_i, v_j\}$ and edges $\{e_1, \ldots, e_k\}$ is reduced to a simple graph withe the same two vertices and a single edge. The resulting edge admittance, $Y_{ij}(\xi)$ is of the form $G_{ij} + C_{ij}\xi + \Gamma_{ij}\xi^{-1}$ where each coefficient is nonnegative. Doing this reduction for all multiple edges in the full pseudograph reduces the topology to a graph. In particular, the circuit described on this graph has 'elements' of the form $Y_{ij}(\xi)$ described above on its edges. We note that each of these 'elements' are positive real (pr) functions. Summarizing:

Theorem 2: The manifest behavior for an RLC circuit where each vertex is connected to a terminal is represented by $I = Y(\xi)V$ where $Y(\xi) = G + C\xi + \Gamma\xi^{-1}$ where G, C and Γ are symmetric, hyperdominant matrices with zero excess. Conversely, for every such matrix, there exists an RLC circuit with these terminal potential/current behavioral equations.

B. Simple Graph reduction

The second step in obtaining the manifest behavioral equations when not every vertex links to a leaf (terminal) now follows by eliminating terminals in the description of Theorem 2. For instance, if the last vertex is to be 'internalized', we set in

$$I = Y(\xi)V$$

where $\dim I = \dim P = n$, then set $I_n = 0$ and eliminate P_n. Partitioning $Y(\xi)$ as

$$Y(\xi) = \left[\begin{array}{cc} \hat{Y} & -y \\ -y' & y_n \end{array}\right] \tag{10}$$

and setting $I^T = [\hat{I}, I_n]$ results in the Schur complement (reduced) behavioral description

$$\hat{I} = [\hat{Y} - yy'/y_n]\hat{V}. \tag{11}$$

Also note that, with $\mathbf{1} = [1, \ldots, 1]^T$, the column sum property is expressible as

$$\hat{Y}(\xi)\mathbf{1} = y(\xi) \tag{12}$$

$$y'(\xi)\mathbf{1} = y_n(\xi). \tag{13}$$

It readily follows from (12) and (13) that $[\hat{Y} - yy'/y_n]\mathbf{1} = 0$. Hence the matrix in (11) is symmetric and its rows and columns sum to zero. Unless y_n is not a function of ξ, corresponding to a purely resistive edge element, the behavioral equations are no longer described by three symmetric hyperdominant matrices with zero excess.

However symmetry and zero sum properties are preserved throughout each single reduction. Hence, we conclude that the manifest behavioral equations for an RLC circuit are given by $\hat{I} = \widehat{Y}\hat{V}$, where $\widehat{Y}$ is symmetric with row and column sums equal to 0. But is there more structure?
Since the off-diagonal elements in (3) are the negative of positive real functions, one might conjecture that this property is preserved. However, this is false! (See further).

Definition A matrix $Y(\xi)$ is positive real (pr) if $x^*Y(s)x$ is a pr function for all $x \in \mathbb{C}$.

Lemma 3: If a rational $N \times N$ matrix $Y(s)$ is symmetric and pr, then its Schur complements are symmetric, and hyperdominant with zero excess on the positive real axis.
Proof: similar to the resistive case.

Note that if $Y(\xi)$ is pr, then, by definition $x^*Y(\xi)x$ is a pr function for all $x \in \mathbb{C}^n$. Consequently, $x^*Y(\sigma)x \geq 0$ for all real nonnegative σ. This implies that $Y(\sigma)$ is positive semi-definite and symmetric. The Schur complements, Y_{sc}, of such matrices are also symmetric and positive definite: $z^*Y_{sc}(\sigma)z \geq 0$.

But are these conditions also sufficient? Could a necessary and sufficient condition for an $N \times N$ matrix to be the terminal admittance of a passive RLC circuit be that Y is symmetric, p.r zero excess, hyperdominant for real ξ (non-diagonal elements of $Y(\xi)$ nonpositive for real $\xi \geq 0$.)?

Remarks
(1.) It is still unknown which conditions are sufficient. For a resistive network, we have necessary and sufficient conditions.
(2.) Positive realness of the $-\widehat{Y}_{ij}$ for $i \neq j$ is not a necessary condition. Consider the following counterexample. The full

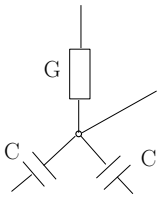


Fig. 3. Y to Δ

behavioral description of this four terminal circuit is $I = YP$ with, for simplicity letting $G = 1$ and $C = 1$

$$Y = \begin{bmatrix} 1 & & & -1 \\ & \xi & & -\xi \\ & & \xi & -\xi \\ -1 & -\xi & -\xi & 1+2\xi \end{bmatrix}. \qquad (14)$$

We want to eliminate the terminal incident to the center of the Y-circuit. The corresponding Schur complement is

$$\frac{1}{(1+2\xi)} \begin{bmatrix} 2\xi & -\xi & -\xi \\ -\xi & \xi^2+\xi & -\xi^2 \\ -\xi & -\xi^2 & \xi+\xi^2 \end{bmatrix}. \qquad (15)$$

The (2,3)-element is

$$-\frac{\xi^2}{1+2\xi}.$$

Its real part evaluates on the imaginary axis to

$$\Re Y_{23}(j\omega) = \frac{\omega^2}{1+4\omega^2}.$$

Hence $-Y_{23}(\xi)$ is not a pr function. The interpretation of (15) is as the admittance matrix of the Delta in the Y-Δ transformation. The admittances in the edges of the Delta are thus not all positive real functions!

V. Conclusion

We have shown how the behavioral equations for a purely resistive circuit with time invariant resistors may be extended to an RLC circuit with linear time-invariant elements. The behavior is represented by a rational matrix in ξ which is symmetric, positive real and with zero column and row sums. Its evaluation on the positive real axis is hyperdominant with zero excess. We have also shown that the full extension (notably the converse) of Theorem 1 for purely resistive networks is far from trivial. In particular the quest for sufficient conditions is still open.

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